Design of Charge Pump for Wireless Energy Harvesting at 915 MHz

Senior Capstone Project Report

By: Mark McKean and Milko Stoyanov

Advisors: Dr. Brian Huggins and Dr. Prasad Shastry

Department of Electrical and Computer Engineering

Bradley University

Peoria, IL 61625

2017

BRADLEY University

PANDUIT®

Abstract

Panduit, a manufacturer of communication infrastructure products, requested a receiver be designed and implemented to harvest wireless RF energy to power remote sensors. In the first iteration, the RF signal will be transmitted from a base station operating at 915 MHz with future iterations using the RF energy in the digital TV bands.

This report describes the design, simulation, and implementation of multiple RF-DC charge-pump circuits. Recent published literature describes the efficacy of such topologies for RF energy harvesting. Both a 2-stage charge-pump and a 5-stage charge-pump, optimized for different incoming power levels, are presented. These circuits, consisting of matching circuits, diode-capacitor stages, and a load, were designed and simulated using SPICE® and ADS®. The microstrip circuit boards were fabricated by Micro Circuits based on ADS® designs and components inserted by the team members. The report compares simulated results to experimental results.

Acknowledgements

We would like to thank our advisors Dr. Brian Huggins and Dr. Prasad Shastry for their excellent guidance and helpful support with this project.

We would like to thank the entire Electrical Engineering Department for teaching us the skills and knowledge necessary to be successful in this project.

We would also like to give a special thanks to our lab director Mr. Christopher Mattus for ordering our supplies and a special thanks to our assistant lab director Mr. Nick Schmitt for teaching us how to solder small components.

We would like to thank Micro Circuits for fabricating the circuit boards for this project.

We would also like to thank Panduit® for sponsoring this project.

Table of Contents

Chapter 1

Introduction

Wireless energy harvesting opens up a new world of possibilities in the field of electrical engineering with applications in consumer electronics, aerospace technology, and systems that cannot be reached by wires. In certain applications a wired connection is simply not practical. Wireless energy is already in the air around us, and it could be harnessed for power.

The applications for this field of study are vast. One application involves harvesting energy from sources already present in the environment. Another application involves transmitting an RF signal from a controlled source, which is known as wireless power transfer. Traditionally these systems are powered by a receiving antenna that is in turn getting power from a transmitting antenna.

Any operation that uses rechargeable batteries could benefit from wireless energy harvesting. Instead of having to replace the dead batteries, they could be outfitted with an RF energy harvester that converts RF energy into DC, and recharges the batteries. A nearby substation would be the source of the RF energy that could be activated when the need arises. The designs in this paper utilize a signal generator that is directly connected to the circuit in place of a receiving antenna in order to simplify the engineering process. The signal will be of a varying power level at a frequency of 915 MHz. This project lays down the ground work for using a charge-pump to convert RF energy to DC energy. Both a 2-stage and 5-stage charge pump were designed for different input power levels.

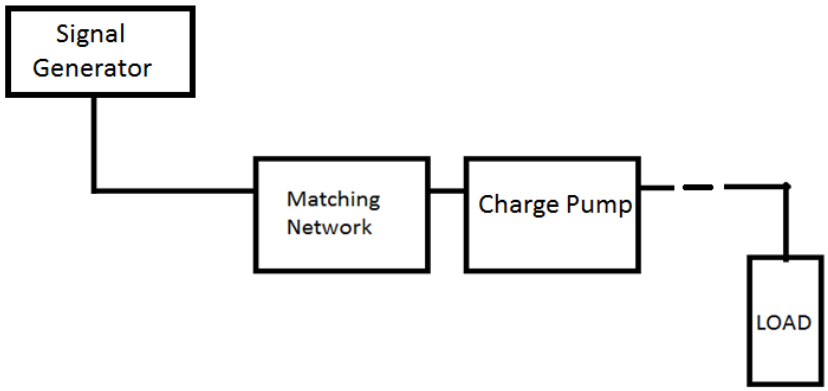


Fig 1.1. System Block Diagram

In Fig. 1, the load will consist of a parallel RC network, however for each design a circuit without a load was also designed and fabricated. The signal generator will supply power levels of -20, -10, and 0 dBm at 915 MHz. There will be a unique matching network for each power level in both the 2-stage and 5-stage designs, in order to maximize the transfer of RF energy to the charge-pump. In the chapters to follow, the designs, simulation results, and experimental results will be presented.

Chapter 2

Literature Review

2.1 Introduction

This section of the report will discuss prior work in the field of wireless energy harvesting in published literature.

2.2 Parametric Analysis and Design Guidelines of RF-to-DC Dickson Charge Pumps for RFID Energy Harvesting [1]

In this paper the authors used MATLAB to simulate a Dickson charge-pump for low RF input power. The paper looked at each of the design parameters and the considerations for choosing optimal values. A step-by-step process for designing a rectenna was included along with a list of general guidelines. The design used Skyworks SMS7630 diodes. After analyzing results, it was determined that any more than 2-stages will not reliably increase efficiency. However, adding stages can increase output voltage if the output resistance and input power are large. This was only done in simulation and did not have any experimental results to compare with simulation.

2.3 Ambient RF Energy-Harvesting Technologies for Self-Sustainable Wireless Sensor Platforms [2]

This review paper discusses the applicability of energy harvesting technologies. It goes into some detail about other methods of energy harvesting including solar, thermal, and piezoelectric, but focuses primarily on Radio Frequency signals. This paper confirms that it is possible to produce a useful amount of power from a passive rectenna system. It also contains graphs and tables of energy density of different frequency bands in multiple urban environments which is a helpful reference for the sake of comparison to conditions in the laboratory. Furthermore, the paper discusses the design considerations of the antenna and rectifying circuitry which will undoubtedly be a useful reference at that point in the design process. An RF to DC charge-pump is detailed in the paper.

2.4: Ambient RF Energy Harvesting in Urban and Semi-Urban Environments [3]

In this project, RF spectrum measurements were taken in several underground stations in London. The largest power contributions came from the following systems: DTV, GSM900, GSM1800, and 3G. This was before 4G became operational. The measurements were made using the Hold function, in order to measure the largest a signal at certain frequencies. A prototype was designed and used for each band. A linear polarized folded dipole antenna was selected for use. A modified folded dipoles was used to get a good input impedance of 50 ohms, and a balun was not necessary. The Skyworks SMS7630 diode was used in the rectifier. An output capacitor in parallel with a load resistor was used. The capacitor needs to be less than 1 pF in order to have a good shunt match.

2.5 E-WEHP: A Batteryless Embedded Sensor-Platform Wirelessly Powered From Ambient Digital-TV Signals [4]

In this project, an optimized log-periodic antenna, an RF-DC charge-pump circuit, and an embedded firmware have been developed to sustain embedded microcontrollers at long range from digital TV signals. This paper shows that energy harvesting is suitable for a variety of applications. Relevant to this report, the paper also details an RF-DC charge-pump, designed using Keysight's Advanced Design System (ADS). It also includes a discussion on how the charge-pump functions.

2.6 Smooth Moves in Power Transition [5]

A contest was held to develop an antenna with a rectifier circuit. The RF Power in a Linear, vertically polarized signal at 2.45 GHz was to be transformed into DC power. An input of 1 uW/cm^2 was to be used to generate at least 10 uW of DC power. There was a weight limit, and the design had to be two dimensional, with a height of no more than 5mm for the antenna. The rectifier was a half-wave rectifier with an inductor in series. Initially a Skyworks SMS7630 detector diode was used, but was later replaced with an Avago HSMS-285Y in order to have slightly higher output power. This was not seen in simulation and could just be coincidental. The impedance of the signal source was 50 ohms, the optimal load resistance was determined to be 2250 ohms, giving the highest measured efficiency of 56% when a constant input power of -6 dBm was used. A Yagi-Uda antenna was used in order to fit into the contest parameters. This gave the best results for the contest.

2.7 Concluding Remarks

The preceding literature proved to be a valuable source of information for this project. Much of the design process for this project was structured by the guidelines given in papers [1] and [2]. The following section will discuss the design of the system.

Chapter 3

Design of Charge-Pump

3.1 Introduction

This section of the paper will discuss the design process in chronological order beginning with the selection of the load, then the charge pump as well as the considerations for diodes, followed by the microstrip implementation and layout, and finally the matching network.

3.2 The Load

To begin the design process, first a load must be chosen. Other papers on this subject have used a load with a high resistance to replicate the conditions of microcrontrollers that could be used in energy harvesting applications. One paper claims that the DC Load resistance dramatically affects both efficiency and input impedance; the output capacitance has a negligible effect on the charge-pump RF-DC conversion efficiency [1]. However, a larger capacitor increases the time it takes to charge. Also, a larger capacitor minimizes output voltage ripple. With these considerations in mind, it was decided that this project would use a load of 1 MΩ in parallel with a 1 µF Capacitor, as shown below in figure 3.1.

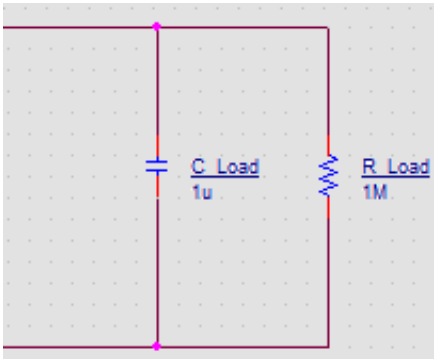


Fig. 3.1. Parallel RC Load

3.3 The Theory of Charge-Pump

An N-Stage Charge-pump schematic is shown in Fig. 3.2. Charge-pumps function in the following way. During the negative half-cycles, odd numbered capacitors get charged to a voltage equal to the input RF signal, on the right side of the capacitors, plus the voltage across the preceding even numbered capacitors through odd numbered diodes, minus the forward voltage loss across each diode. Even numbered capacitors get charged in a similar way through even numbered diodes, during positive half-cycles. Because of the nature of diodes, where current flows from anode to cathode, they act as a one way valve, preventing the charge flowing back through the diodes.

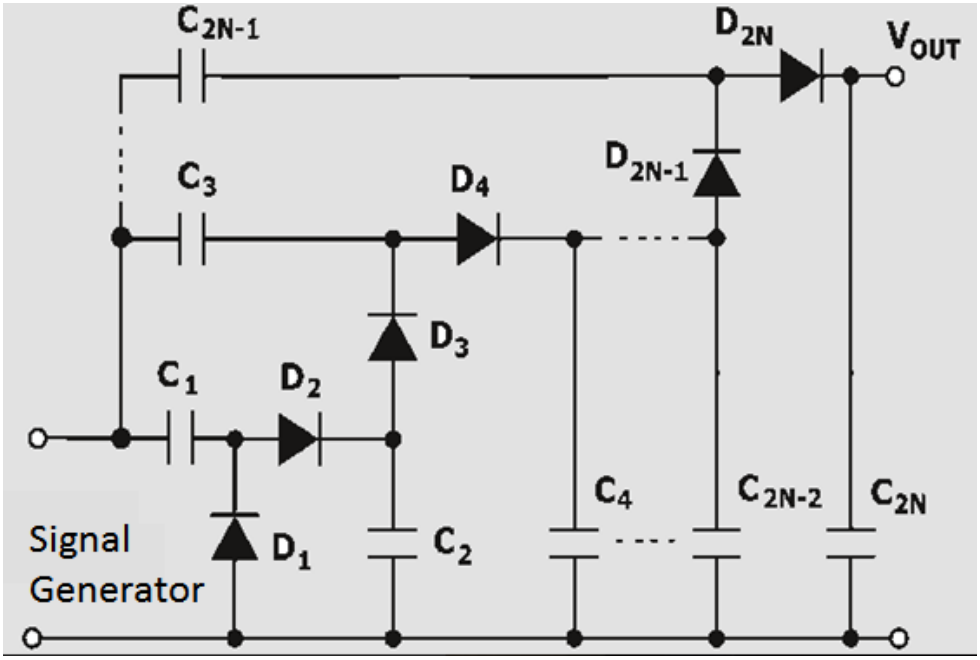


Figure 3.2. N-Stage Charge Pump Schematic

3.4 The Diode

The most crucial component of the charge-pump is the diodes. After reviewing related works, it was observed that only two types of diodes were used in their designs. These specific diodes were appropriate for low power RF applications, because they have a lower knee voltage than other diodes. The knee voltage is the point where a diode starts conducting. The input power must be sufficient to forward bias the diodes, less power is needed for a diode with a lower knee voltage. If the diodes do not become forward biased, no rectification will take place. Without rectification the circuit fails to perform it's intended operation.

Also, the non-linear nature of diodes proved to be a source for complexity and difficulty in the design process. The non-linear nature of the diode causes the input impedance to change as a function of input power. Because of this, the matching network must be different depending on the input power level the circuit is designed for.

The two RF diodes that were used in related papers were the Avago HSMS 2860 and the Skyworks SMS7630. Both of the diodes were simulated in a simple circuit shown in Figure 3.3, done in ADS®. The data sheet parameter values for each diode, provided on the manufacturers' websites (APPENDIX A), were copied into the diode model block in ADS®. The I-V characteristics were obtained from the above circuit. It is evident from Fig. 3.4 and Fig. 3.5, the output of Fig. 3.3, that the Skyworks diode has a lower knee voltage, which made it better suited for low power applications.

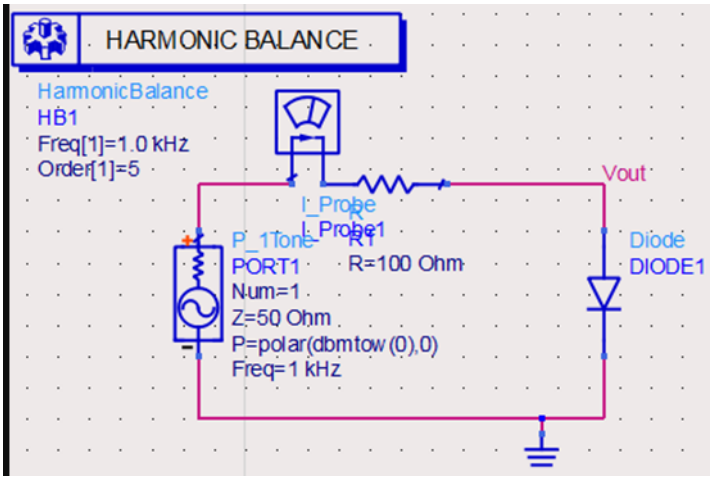


Fig. 3.3. Diode testing circuit

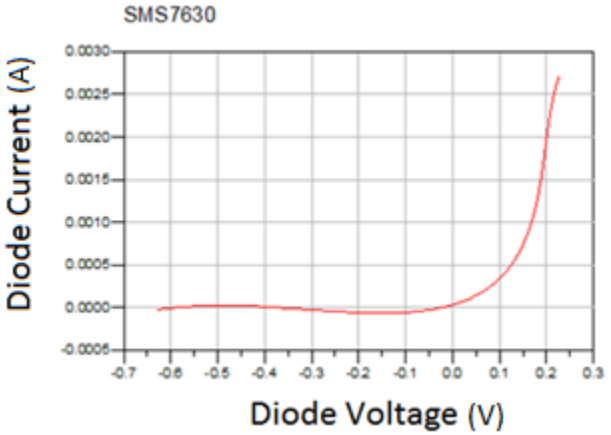


Fig. 3.4. I-V Characteristic of Skyworks SMS7630

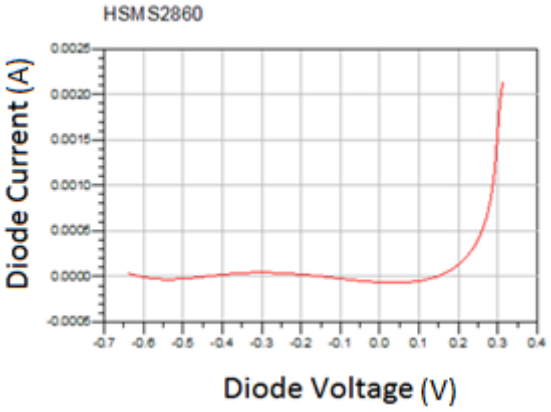


Fig. 3.5. I-V Characteristic of Avago HSMS2860

3.5 Topology of the Charge-Pump

It was determined that two different topologies would be designed for the sake of comparison. One paper reviewed for this project mentioned a 2-stage topology being the most efficient at low input power levels [1]. Also the paper mentioned that more stages can increase the output voltage given the right conditions. Another paper used a 5 stage charge pump to power a microcontroller that required a voltage larger than 1.8V [2].

In order to compare the performance of both topologies, designs were made for three different input power levels. The only difference in the designs was the matching network that is detailed in a later section of this report. For each power level, two layouts were designed, one with an on-board load, and one with a connector that could be connected to any load. The on-board load was capacitor and resistor in parallel. The schematics for both a 2-stage and 5-stage are shown in Fig. 3.6. and Fig. 3.7.

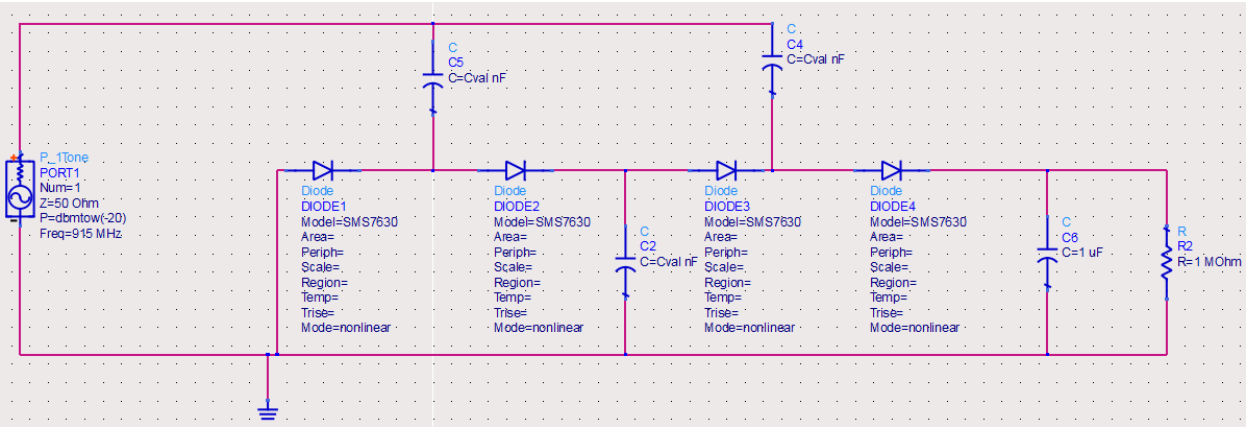


Fig. 3.6. 2-stage charge-pump with load

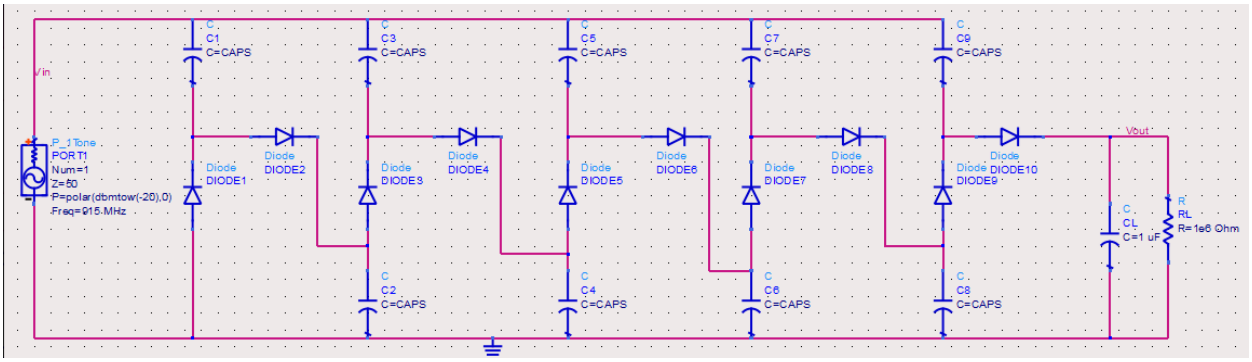


Fig. 3.7. 5-stage charge-pump with load

3.6: Capacitors in the Charge-Pump

The charge-pump capacitors affect the charge-rate of the circuit. With a larger capacitance, it will take longer for the output voltage to reach DC steady state. In this application, the charge-rate is not an important consideration due to not having specified time constraints. According to one paper: “Stage capacitance size appears to have little effect on efficiency”. In the same paper, they claim that the stage capacitance should be large enough to have a low impedance at RF frequencies, greater than 3pF being sufficient [1]. This was used as the starting point for this parameter value. The circuits in Fig. 3.6. and 3.7. were used to sweep the values of stage capacitance, it was found that a standard value of 100nF gave good results. However, the impact of changing this capacitor value proved to be not substantial.

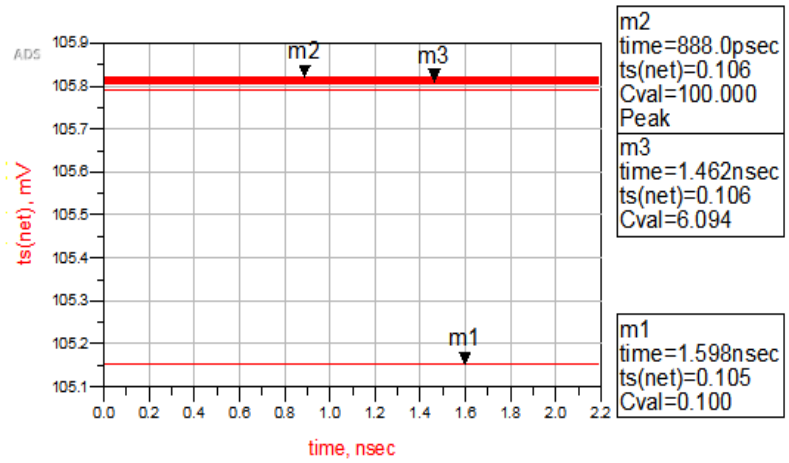


Fig 3.8. Output voltage of 2-stage charge-pump with swept values of capacitance

3.7 Layout of the Charge-Pump Circuit

Before creating a matching network, a microstrip circuit was implemented. This was done to take into account the losses and other effects introduced in the creation of the circuit that are not present in lumped-element circuit simulations.

To begin this process, properties of the substrate and microstrip was determined. The first consideration for this is to decide the on the substrate material. It was decided that the boards would use FR-4 substrate, having a dielectric constant of 3.9. The next consideration was the desired microstrip width for a characteristic impedance of 50Ω. This is because the microstrip width should be comparable to the size of the components that will later be soldered onto it in order to minimize discontinuities. From a list of possible choices, a height of 24 mils was chosen for the substrate, leading to a microstrip width of 1.275mm which is close to the diode width of 1mm. This width was calculated using the MSTRIP program available in the RF Laboratory.

After determining the board parameters, a Layout was created with the exact measurements of the connections between components. The Layout feature in ADS allows the user to place microstrip pieces, along with information on the material, width, and length of these pieces, and arrange them to form the actual circuit. In a layout, gaps are left to represent the space that will be occupied by components.

The main purpose of a layout is that it allows the circuit to actually be fabricated. The layout file, a gerber file (.gbr), along with information about the dimensions and characteristics of the substrate and conductor, was sent to circuit board manufacturers. The reason that the

layout must be determined before the matching network is because the microstrip lines affect the input impedance of the circuit. For both the 2-stage and 5-stage circuits, layouts were created with a couple of considerations in mind. The first being to keep the board small, as applications of this device may require it to fit into small spaces. The second consideration was to keep components far enough away from each other to ensure that they are not interacting with one another in an undesirable way, as well as making soldering less challenging. The layouts, pre-matching network, for both the 2-stage and 5-stage charge-pumps with on-board loads are shown in Fig. 3.9. and 3.10. The holes present in the layout represent via holes, which are used to connect the circuit to ground.

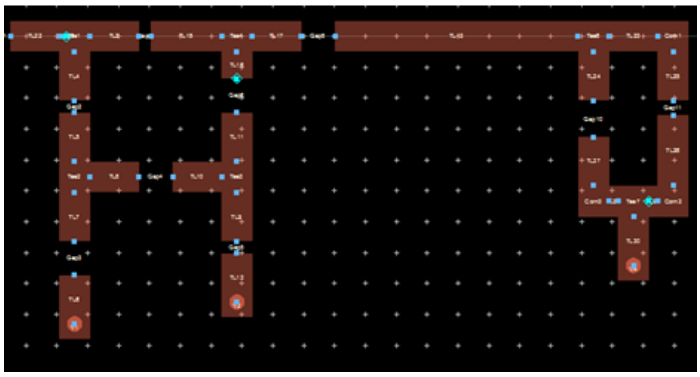


Fig. 3.9. Layout of 2-Stage charge-pump with on-board load (not to scale)

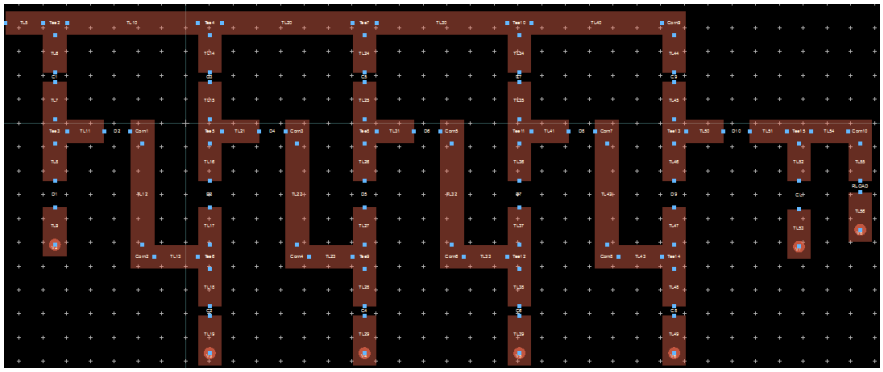


Fig. 3.10. Layout of 5-Stage charge-pump with on-board load (not to scale)

With the layouts created, the details of the layout were added back into the simulation schematic so that the losses and other factors can be taken into account. This was done using microstrip blocks in ADS along with one block that defines the substrate for the entire circuit. The new schematics are shown in Fig. 3.11. and 3.12.

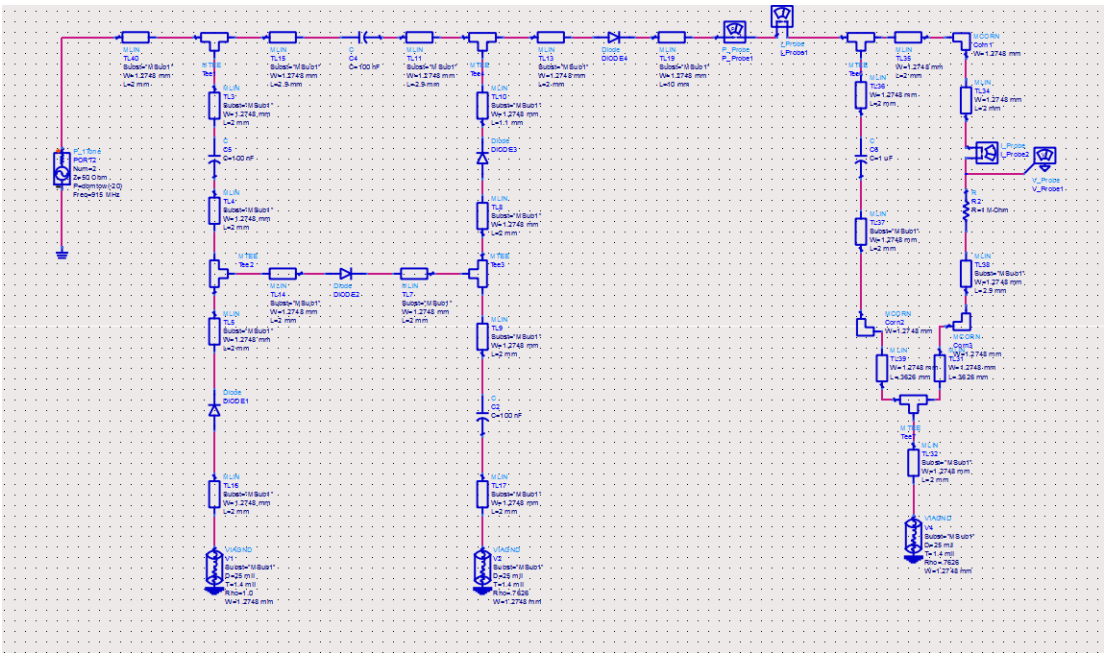


Fig 3.11. 2-stage charge-pump schematic with on-board load and microstrips

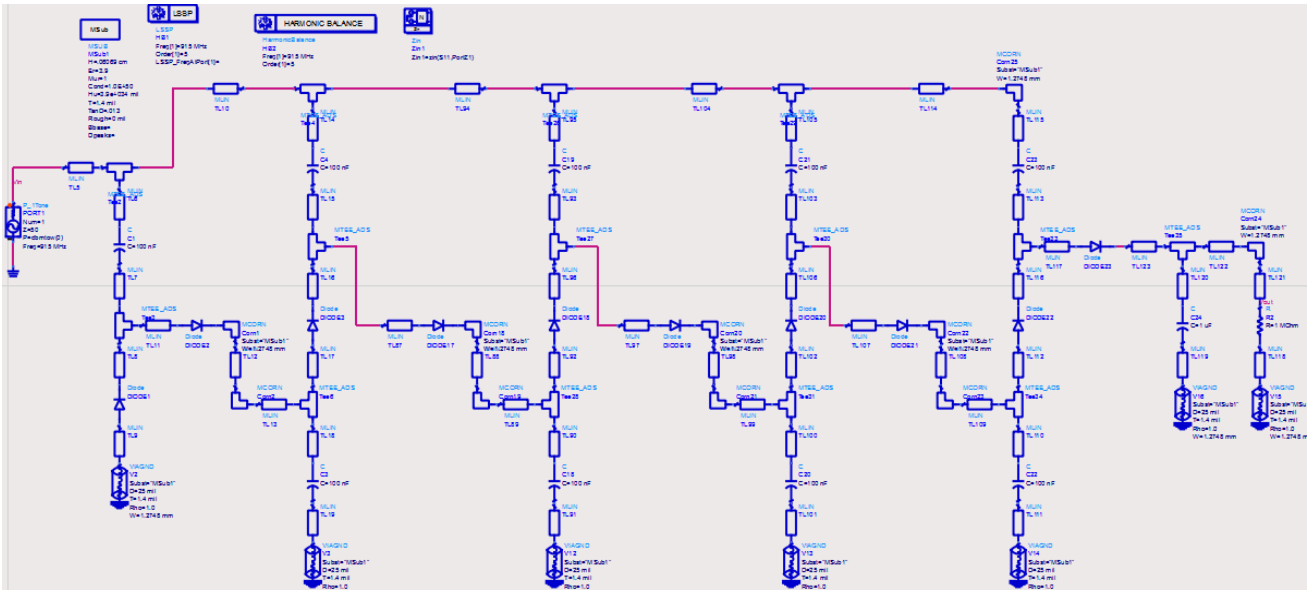


Fig 3.12. 5-stage charge-pump schematic with on-board load and microstrips

3.8 Matching Network Design

The purpose of a matching network is to change the input impedance of a circuit to be equal a desired value. This allows for maximum power transfer into the system by reducing the amount of power that is reflected. There are multiple methods for matching including lumped-element matching and distributed element matching, however, at 915 MHz, distributed element matching is not practical because the circuits would be much larger, as wavelengths are rather large. Lumped-element matching involves series and shunt components consisting of capacitors and inductors.

The input impedance of the circuit must be determined in order to match the circuit to the desired impedance of 50 Ω. To determine the input impedance, the circuits (Figs. 3.11 and 3.12) were simulated using the S-parameter simulation in ADS® as shown in Fig. 3.13. After running an S-parameter simulation, the Zin block can be used to calculate the input impedance. The 5-stage input impedance is shown in Fig. 3.14. Due to the non-linearity of the diodes, Zin changes with input power.

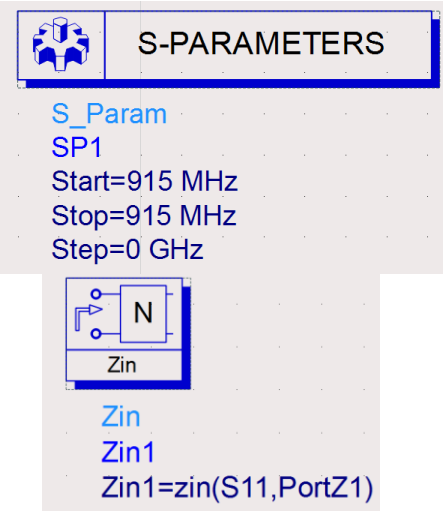


Fig. 3.13. ADS Simulation Blocks

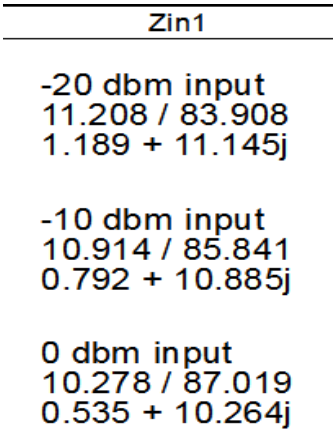


Fig. 3.14. Input impedance of 5-stage charge pump at various power levels

Using the computed input impedance, the circuit was matched to 50 Ω. The MATCH program available in the RF Laboratory was used to calculate a matching circuit for each charge-pump circuit. The matching network element design for the 5-stage charge-pump designed for -20 dBm input power are shown in Fig. 3.15.

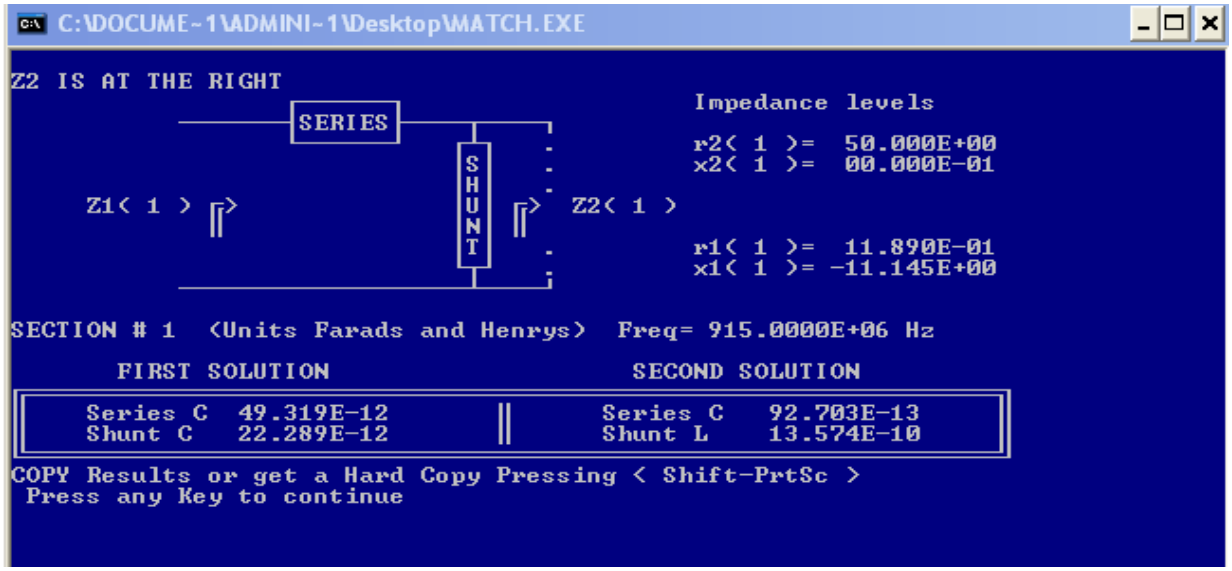


Fig. 3.15. MATCH program output for 5-stage charge-pump (-20 dBm design)

The values displayed in the solution boxes in Fig 3.15 will provide a perfect match in an ideal setting, however this is not the case. The microstrip pieces that make up the connections in the matching network will also introduce unforeseen effects. First, the microstrip pieces must be added to the layout. After adding the microstrip pieces to the layout, they must also be entered back into the simulation schematic. This introduces parameters that cannot be factored in by the MATCH program.

Using the MATCH program values as a starting point, the component values in the matching circuit were swept to observe any potential changes in the output. The component

values that yield the highest output voltage were to be used for the design. When ordering materials, the values had to be changed again based on the values of real capacitors and inductors that are commercially available. These new values were entered back into simulation, and found that the output did not changed significantly.

3.9 Final Designs

This concludes the design of the circuit. The final schematics and layouts of one 2-stage charge-pump and one 5-stage charge-pump are shown in Fig. 3.16 to Fig. 3.19. Only one design of each is shown because the other designs, for different input power levels, only have a different matching network and need not be shown.

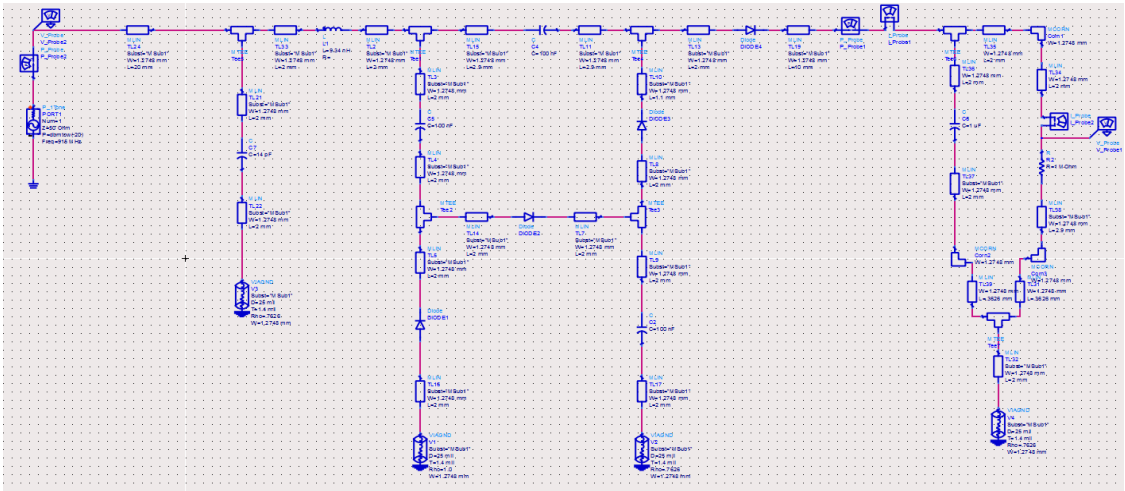


Fig. 3.16. Complete schematic of 2-stage charge-pump designed for -20 dBm input

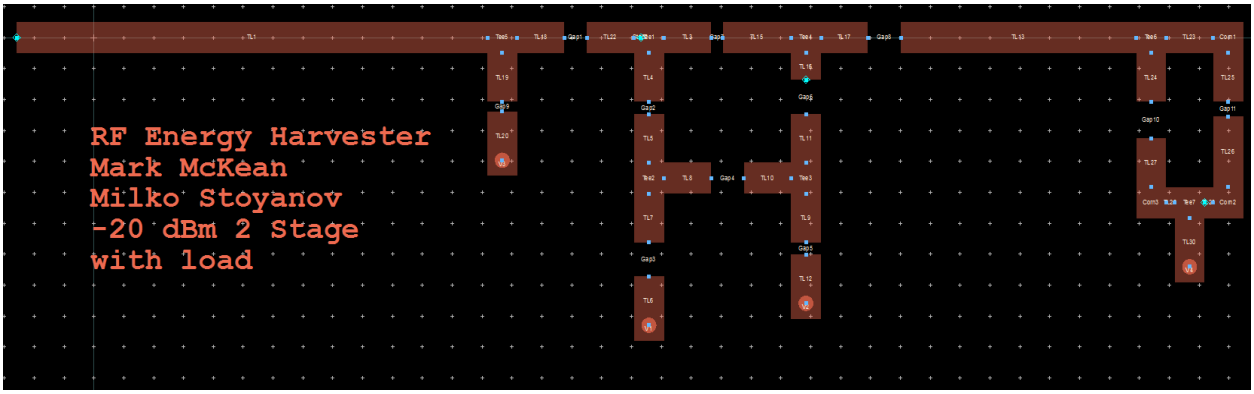


Fig. 3.17. Complete Layout of 2-stage charge-pump designed for -20 dBm input

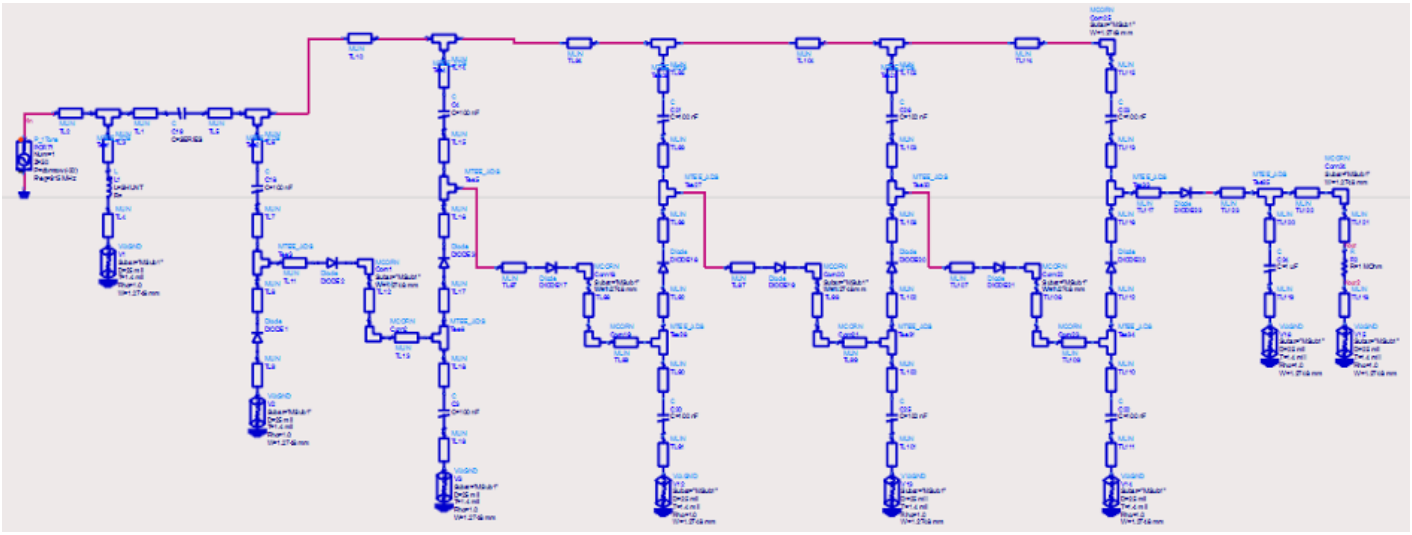


Fig 3.18. Complete schematic of 5-stage charge-pump designed for -20 dBm input

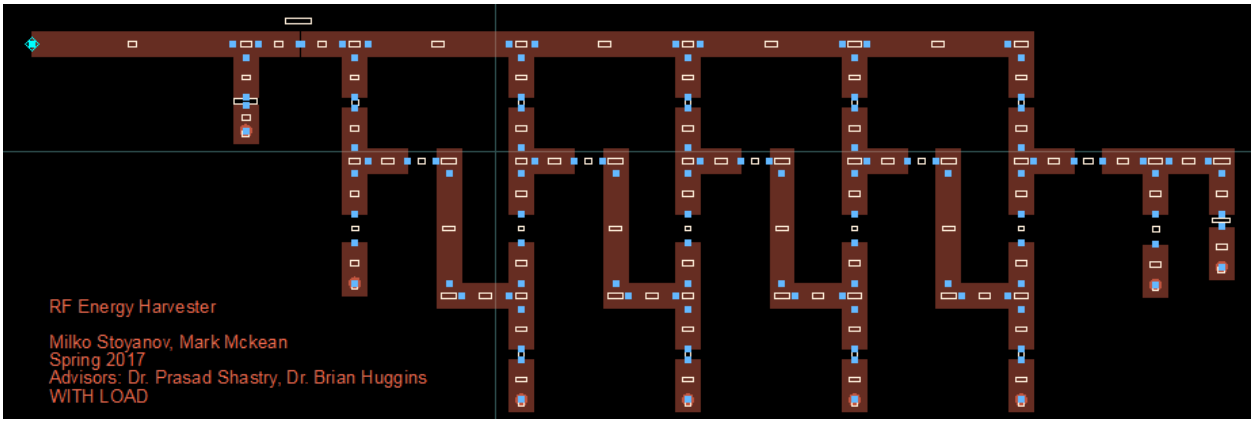


Fig 3.19. Complete Layout of 5-stage charge-pump designed for -20 dBm input

3.10 Concluding Remarks

The design of these systems is complex and requires careful attention to detail and an understanding of each block in order to create the final product. The next chapter of this report will discuss the simulation and experimental results.

Chapter 4

Simulation and Experimental Results

4.1 Introduction

This section will present the simulation and experimental results of the project. First, the simulations of the -20 dBm designs, both 2-stage and 5-stage, will be compared. Second, the simulations of the -10 dBm designs will be compared, followed by the 0 dBm designs. After simulations have been compared, the experimental results will be discussed.

The simulations for this project were done using the Harmonic Balance simulation tool in ADS®. This simulation profile is the most appropriate for non-linear RF applications because it allows one to vary the input power and considers harmonics generated in non-linear circuits. This simulation also allows the user to view a time-domain steady state output of the circuit. This was crucial in this project because the overall goal involves observing the output voltage over time, to ensure that it is in fact DC.

4.2 -20 dBm Design Simulation Results

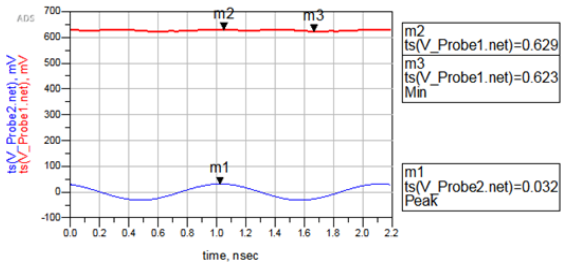


Fig. 4.1. 2-stage (-20 dBm) output voltage compared to input voltage

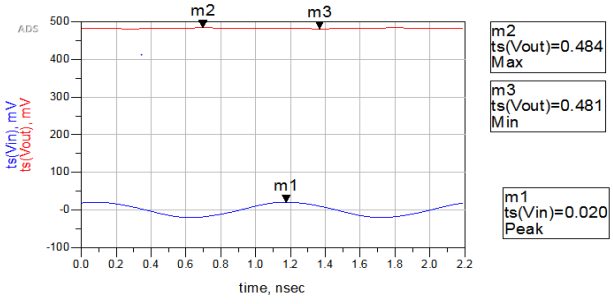


Fig. 4.2. 5-stage (-20 dBm) output voltage compared to input voltage

It is evident from Figs. 4.1 and 4.2 that the 2-stage charge-pump performs better (higher output voltage) under these conditions. The input voltage is different for the 2 designs due to the impedance of the two circuits not being the same, yet having the same input power. The output voltage for the 2-stage is .62 V whereas the output voltage for the 5-stage is only .48 V. This difference could be due to many factors but this does support a claim made in the first paper that a 2-stage charge-pump will perform better at low power levels [1].

4.3 -10 dBm Design Simulation Results

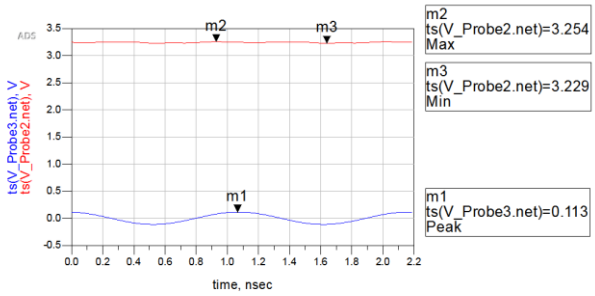


Fig. 4.3. 2-stage (-10 dBm) output voltage compared to input voltage

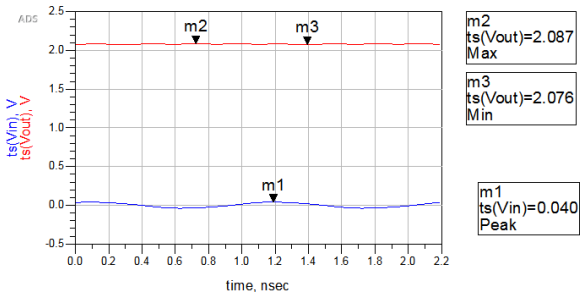


Fig. 4.4. 5-stage (-10 dBm) output voltage compared to input voltage

These graphs are in the same format as the previous simulations. Again, the 2-stage charge-pump produces a higher output voltage for the same input power, implying that the 2-stage charge-pump would be better suited for applications at this power level.

4.4 0 dBm Design Simulation Results

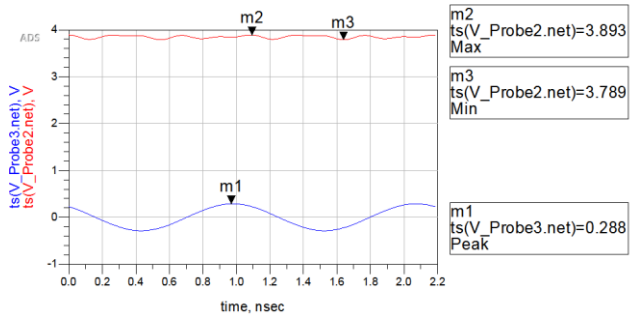


Fig. 4.5. 2-stage (0 dBm) output voltage compared to input voltage

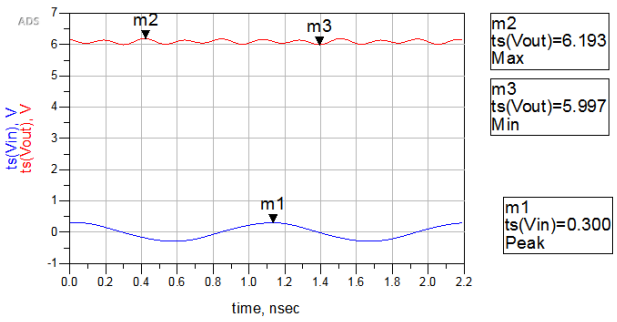


Fig. 4.6. 5-stage (0 dBm) output voltage compared to input voltage

It can be seen in Figs. 4.5. and 4.6. that the 5-stage charge-pump produces a much higher output voltage than the 2-stage charge-pump. Comparing Figs. 4.3 and 4.5, the output voltage barely increased for the 2-stage design. The reason for this is unclear, however, these results support another claim made in the first paper that adding more stages can increase output voltage if output resistance and input power are high [1].

Now that the simulation results have been determined, the next step in evaluating the designs is to build the boards and solder components so that measurements can be taken.

4.5 Building the Circuit

The boards for this project were manufactured by Micro Circuits. For them to produce the boards, they required a layout file in gerber format, as well as a diagram showing the dimensions of the circuit board. Fig. 4.7. and Fig. 4.8. show the boards as they arrived from the manufacturer. The boards shown are the 2-stage -20 dBm designs with and without a load and the 5-stage -20 dBm designs with and without a load.

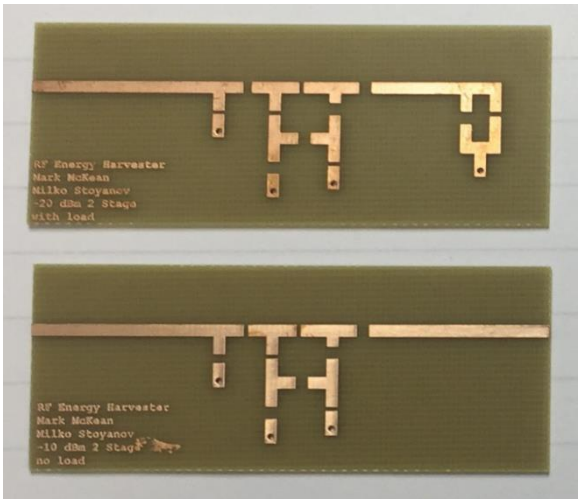


Fig. 4.7. 2-stage boards with load (above) and without load (below)

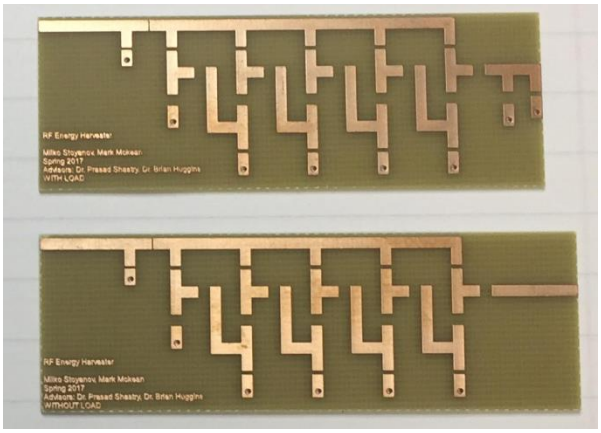


Fig. 4.8. 5-stage boards with load (above) and without load (below)

The background of these photographs is a standard piece of notebook paper, showing how small the boards and component spaces are. With components so small, soldering proved to be quite challenging and time consuming.

With the semester coming to its end, there was not enough time to solder every board. One 2-stage (-20 dBm), one 2-stage (-10 dBm), and one 5-stage (-20 dBm) design were populated with components. These are pictured in Figs 4.9. and 4.10.

Fig. 4.9. 2-stage (-20 dBm) complete circuit (above) 2-stage (–10 dBm) complete circuit (below)

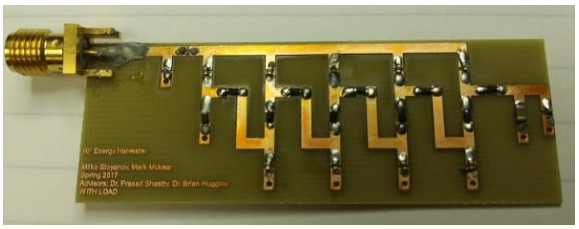
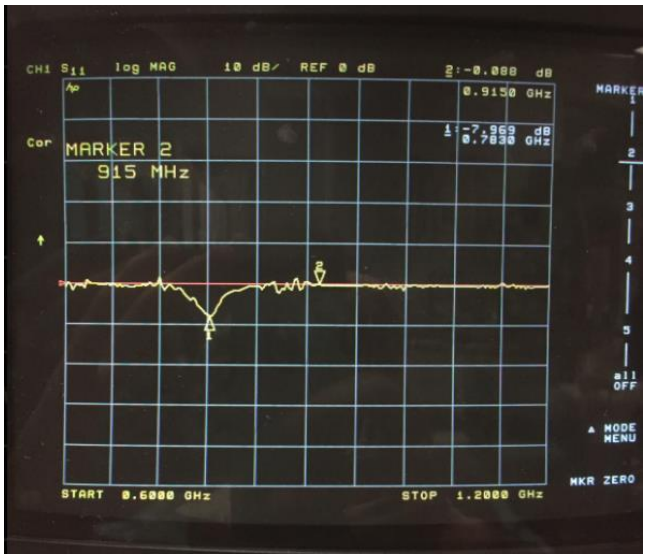
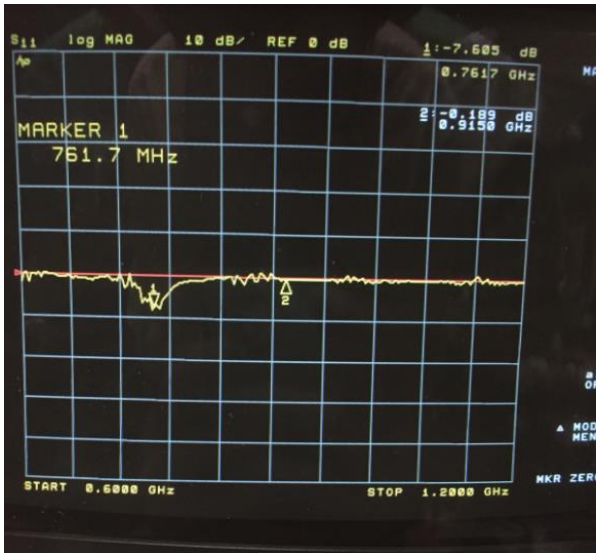


Fig. 4.10. 5-Stage -20 dBm complete circuit

4.6 Experimental Results

From the three boards that were completed, very interesting information was uncovered. After the soldering was complete and the board was checked for continuity and other soldering mistakes, the board was connected to the Network Analyzer which is capable of displaying S_{11}, the reflection coefficient, of the circuit over a given frequency range. Figs. 4.11, 4.12, and 4.13 show the reflection coefficients of the soldered boards.





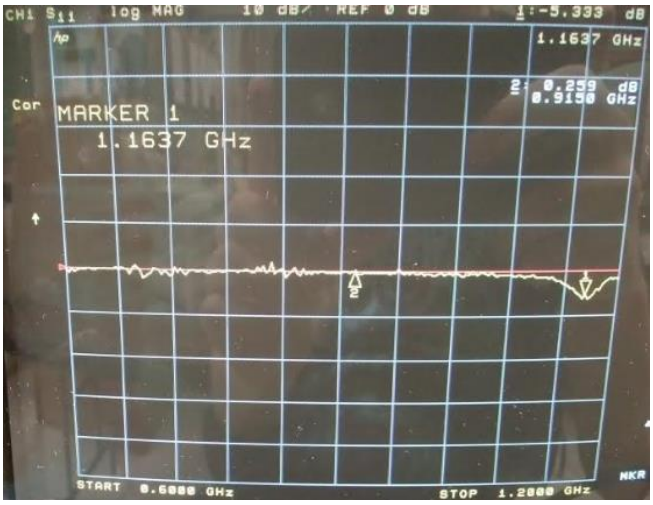


Fig. 4.11. (top left) S_{11} of 2-stage (-20 dBm) circuit board

Fig. 4.12. (top right) S_{11} of 2-stage (-10 dBm) circuit board

Fig. 4.13. (bottom) S_{11} of 5-stage (-20 dBm) circuit board

These figures show some troubling information! It can be seen that the point of lowest reflection coefficient, is not 915 MHz in any of these graphs. Fig 4.11 shows 780 MHz as the optimum frequency, Fig 4.12 shows 760 MHz as the optimum frequency, and Fig 4.13 shows 1.15 GHz as the optimum frequency. The reasons for this are unclear.

After the circuits were tested for S_{11}, they were tested for output voltage. Due to the optimum frequencies not being the same, each circuit was tested at 915 MHz and the optimum frequency. Unfortunately, the 5-stage completed board did not produce any output voltage. The reasons for this are unknown but perhaps due to a soldering mistake or due to not having sufficient substrate surrounding the microstrips on the board, as can be seen in Fig. 4.10. The 2-stage designs were tested and the results are shown in Table 4.1.

Table 4.1

Charge-pump output voltage vs. input power

Board	Frequency (MHz)	Input Power (dBm)	Output Power (V)
-20 dBm input Board	780	-20	0.31
		-17	0.52
		-14	0.83
		-10	1.47
-10 dBm input Board	760	-20	0.228
		-17	0.408
		-14	0.65
		-10	1.2

As can be seen from Table 4.1, the -20 dBm board works better at all incoming power levels, including -10 dBm which the circuit was designed specifically for. One possibility is that the reflection coefficient difference, -8 dB (for -20 dBm board) compared to -7.6 dB (for -10 dBm), may be part of the reason. The output voltage values were found to be smaller in reality than they appeared to be in simulation for each tested board. Figs. 4.14. and 4.15 show the lab setup and a block diagram of the testing circuit.

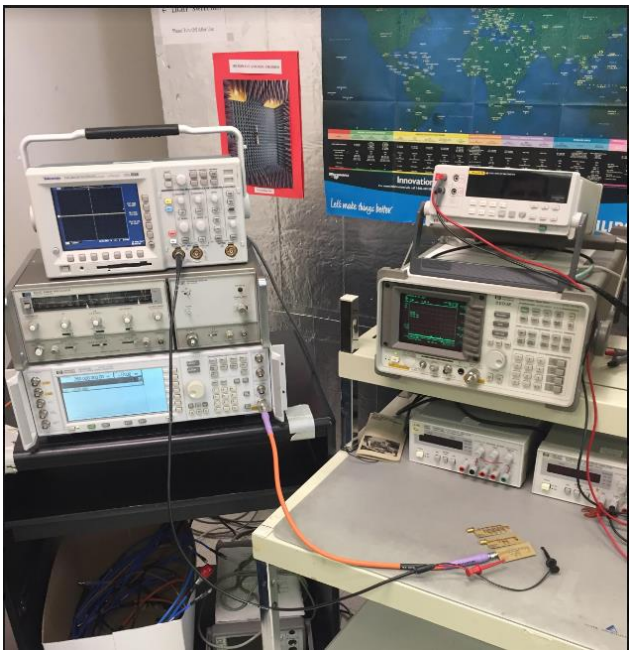
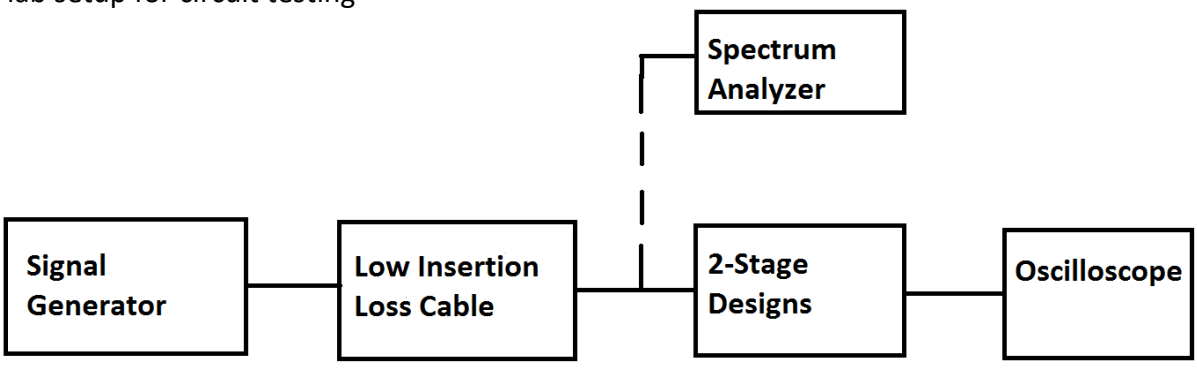


Fig. 4.14. (right) Lab setup for circuit testing

Fig. 4.15 (bottom) Block diagram of lab setup for circuit testing



Chapter 5

Conclusions and Recommendations

There are many projects that could stem from the creation of the 2-stage and 5-stage charge-pump designs. The first of which could be determining why the 5-stage circuit was not able to cive an output. This would require troubleshooting the components, and most likely improvising a solution to the connector problem. If something is considered damaged, it could be removed and replaced, or a whole new board could be carefully soldered with components. Another problem with the design was that the matching network components were incredibly small. A matching network can be designed with larger components that are easier to solder.

The non-linearity of the circuits could be investigated, in order to explain the shift in frequency. All circuits were designed for 915 MHz, but when S_{11} was measured, he best impedance match occurred at a different frequency. The matching network may be adjusted to possibly make a better match to the circuit at the desired frequency.

Another possible project could be designing a 3-stage charge-pump that performs the same function as those presented in this report. This new design could be compared to the 2-stage and the effect of adding an extra stage could be analyzed.

The end goal of this application would be to use an antenna as an RF power reciever instead of a direct connection to a signal source. An antenna like the one used by PowerCast® can be used. The antenna's impedance must be measured, and then the circuit will need a matching network that matches to that antenna instead of to 50 ohms. A further step could be designing an antenna and using that in the system.

APPENDIX A

Guidelines for fabrication.

In order to fabricate the design of a microstrip board, the board manufacturer must know how large the spaces around the microstrips are. Before this happens, lengths of the microstrips themselves, must be correct. An example of what should be prepared is shown in Figure A1.

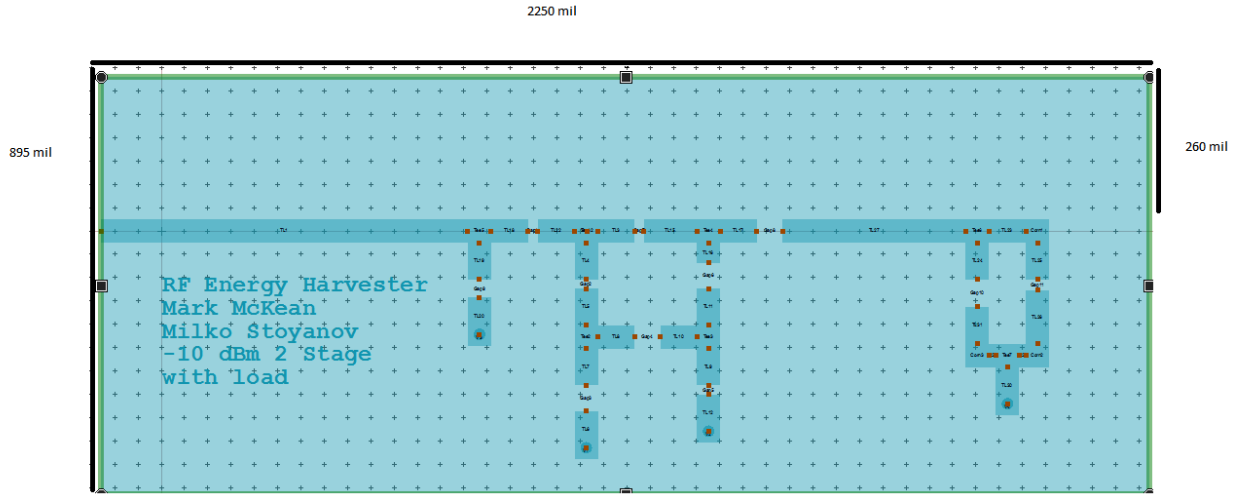


Fig. A1. Example of the 2-stage layout board dimensions

The overall size of the board can be shown in the following way:

1. Use the snipping tool/ take a screenshot then crop it using a program like Microsoft paint.
2. Use a program like Microsoft Paint to draw lines, and use the text tool to write down the dimensions of those lines. The lines do not have to be to scale, but it should be mentioned if the are not to scale.

3. Be sure to leave space above and below the top and bottom of the cicuit. Also make sure wherever a connector is being attached, is right on the edge of the board.

Some mistakes that really hurt the project were made in the 5-stage layour fabrication. Which is shown in Fig. A2.

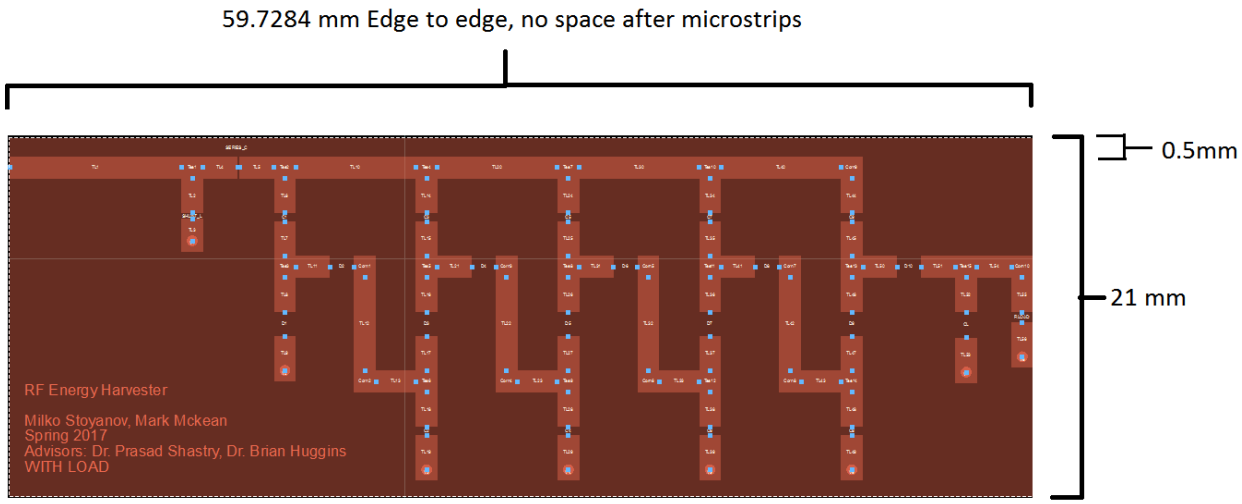


Fig A2. 5-stage layout board dimensions

If there is little to no space above and below the microstrip, it is really difficult to attach a connector, shown in Fig. A3. Also, a minimum width (3 times the microstrip width) of ground plane is neccesary for microstrips.

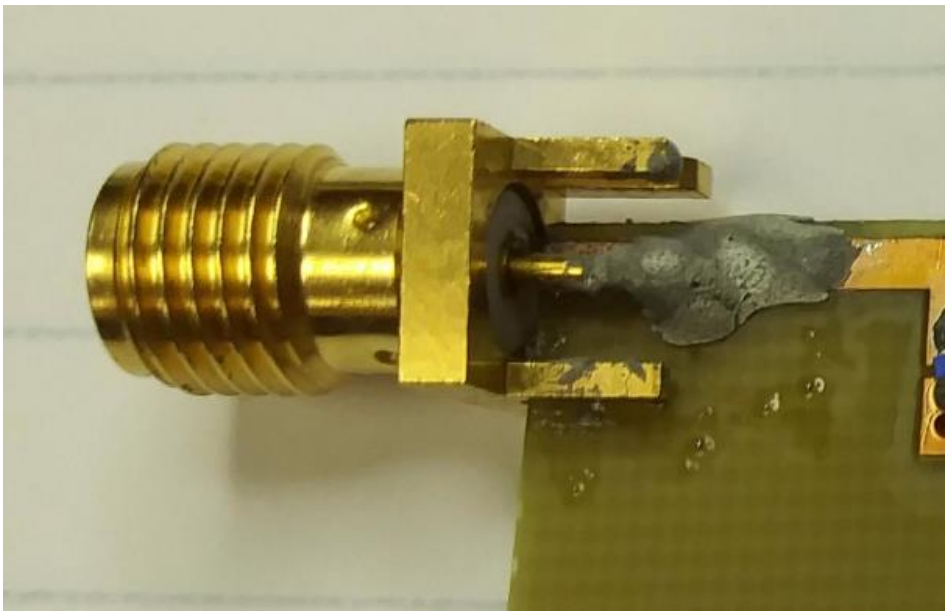


Fig. A3. Connector that was attempted to be connected to 5-stage circuit board

Additionally, if a heat bath is used for soldering, space is needed in order to hold the board over the bath, while not covering any gaps or parts of the microstrip. Even where a connector will not go, space should be left between the edge of the board and the microstrip.

Another serious problem was using very small components. Although RF surface mount components will be small no matter what, there are some that are slightly larger. If bigger size components can be picked without compromising other parameters, they should be prefered. With tiny components, soldering them becomes more difficult, frustrating, and problematic! The gaps must be determined from the data sheet. If dimensions are not very clear in component schematics, it is better to have a shorter gap rather than a gap that is too long. If the gap is too spread apart, the component cannot be connected at all, and will cause many problems.

APPENDIX B

Skyworks Diode Data Sheet

SKYWORKS®

DATA SHEET

Surface Mount Mixer and Detector Schottky Diodes

Applications

- Sensitive RF and microwave detector circuits
- Sampling and mixer circuits
- High-volume wireless
- WiFi and mobile
- Low-noise receivers in high-sensitivity ID tags
- Radio designs

Features

- Tight parameter distribution
- Available as singles, pairs, and dual pairs
- Packages rated MSL1, 260 °C per JEDEC J-STD-020

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

Description

These low-cost, surface mountable, plastic packaged silicon mixer Schottky diodes are designed for RF and microwave mixers and detectors. They include low barrier diodes and zero-bias detectors that combine Skyworks advanced semiconductor technology with low-cost packaging techniques. All diodes are 100 percent DC tested and deliver tight parameter distribution, which minimizes performance variability.

These diodes are available in SOD-882, SC-79, SOT-23, and Molded Interconnect System (MIS) packages. Wiring configurations include singles, common cathode, series pairs, unconnected pairs, and dual series pairs. They may be used at frequencies up to 24 GHz.

Table 1 describes the various packages and marking of the mixer and detector Schottky diodes.

Table 1. Schottky Diode Packaging and Marking

					
Single	Single	Series Pair	Reverse Series Pair	Unconnected Pair	Single
SC-79 Green™	SOT-23	SOT-23	SOT-23	MIS Green™	SOD-882 Green™
				SMS7621-517 Marking: H Pb-Free	
◆**SMS7621-079LF** Marking: Cathode and SA	**SMS7621-001LF** Green™ Marking: XH1	◆**SMS7621-005LF** Green™ Marking: XH2	◆**SMS7621-006LF** Green™ Marking: XH8		**SMS7621-040LF** Marking: E
◆**SMS7630-079LF** Marking: Anode and SC		**SMS7630-005LF** Green™ Marking: XD2	◆**SMS7630-006LF** Green™ Marking: XD8		**SMS7630-040LF** Marking: P
L_S = 0.7 nH	L_S = 1.5 nH	L_S = 1.5 nH	L_S = 1.5 nH	L_S = 0.6 nH	L_S = 0.45 nH

The Pb-free symbol or "LF" in the part number denotes a lead-free, RoHS-compliant package unless otherwise noted as Green™. Tin/lead (Sn/Pb) packaging is not recommended for new designs.

DATA SHEET • MIXER AND DETECTOR SCHOTTKY DIODES

Electrical and Mechanical Specifications

The absolute maximum ratings of the mixer and detector Schottky diodes are provided in Table 2. Electrical specifications are provided in Tables 3 and 4. The associated SPICE model parameters are provided in Table 5. A typical detector schematic diagram is shown in Figure 1.

Typical performance characteristics are illustrated in Figures 2 and 3. Package dimensions are shown in Figures 4 to 10 (even numbers), and tape and reel dimensions are provided in Figures 5 to 11 (odd numbers).

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The mixer and detector Schottky diodes are rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C for 5 seconds. They can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Maximum	Units
Reverse voltage	V_R		Rated V_B	V
Forward current, steady state	I_F		50	mA
Power dissipation	P_D		75	mW
Storage temperature	T_{STG}	–65	+150	°C
Operating temperature	T_A	–65	+150	°C
Junction temperature	T_J		+150	°C

[1] Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD HANDLING: *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 3. Electrical Specifications[1]
(T_A = +25 °C Per Junction, Unless Otherwise Noted)

Part Number	Barrier	Minimum V_B @ 10 µA (V)	Typical C_T @ 0 V (pF)	V_F @ 1 mA (mV)	Maximum Pair Configuration ΔV_F @ 1 mA (mV)	Maximum R_T[2] (Ω)
SMS7621 series	Low	2	0.25	260 to 320	10	18 @ 5 mA

[1] Performance is guaranteed only under the conditions listed in this table.

[2] R_T is the slope resistance.

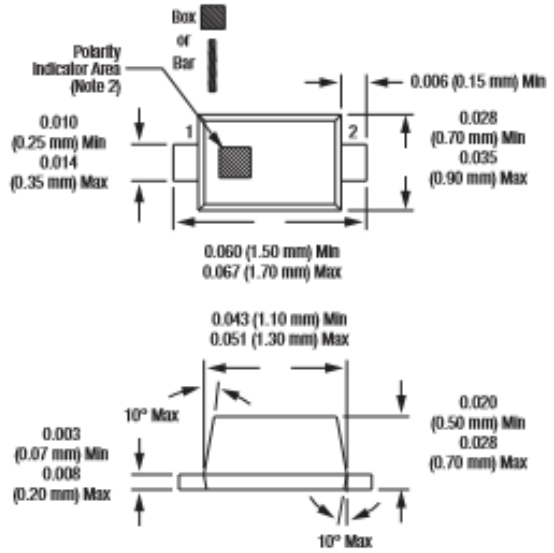
Table 4. Electrical Specifications[1]
(T_A = +25 °C Per Junction, Unless Otherwise Noted)

Part Number	Minimum V_B @ 100 µA (V)	Typical C_T @ 0.15 V (pF)	V_F @ 0.1 mA (mV)	V_F @ 1 mA (mV)	Maximum Pair Configuration ΔV_F @ 1 mA (mV)	Typical R_V (Ω)
SMS7630 series	1	0.3	60 to 120	135 to 240	10	5000

[1] Performance is guaranteed only under the conditions listed in this table.

Table 5. SPICE Model Parameters (Per Junction)

Parameter	Units	SMS7621 Series	SMS7630 Series
I_S	A	4E-8	5E-6
R_S	Ω	12	20
N	–	1.05	1.05
TT	sec	1E-11	1E-11
C_{J0}	pF	0.1	0.14
M	–	0.35	0.40
EG	eV	0.69	0.69
XTI	–	2	2
FC	–	0.5	0.5
B_V	V	3	2
I_{BV}	A	1E-5	1E-4
V_J	V	0.51	0.34

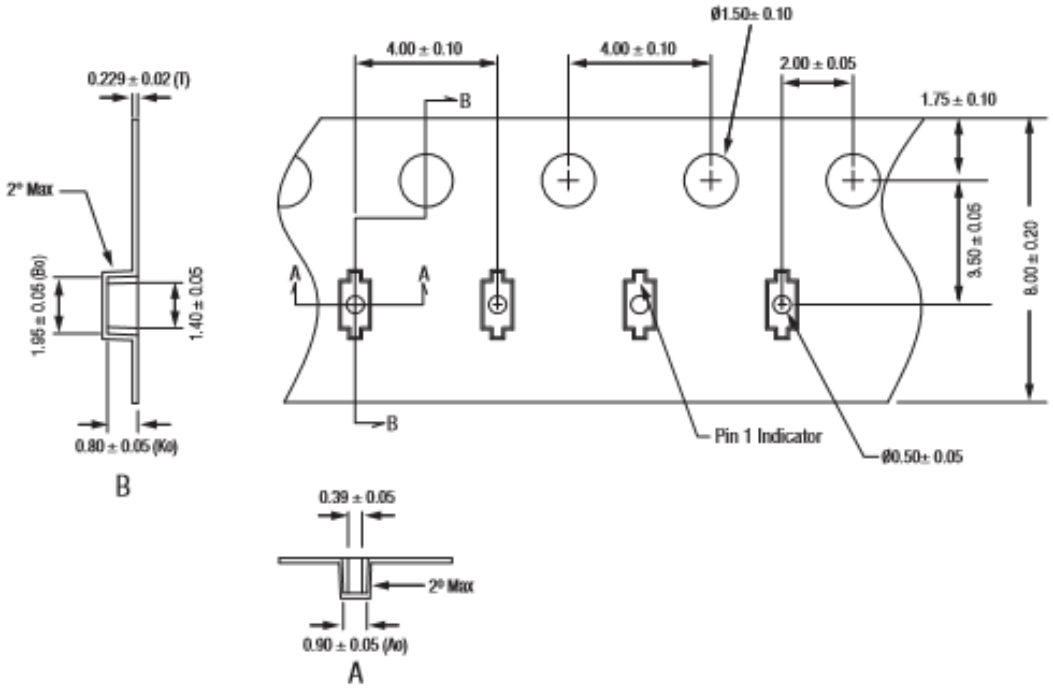


Notes:

1. *Dimensions are in inches (millimeters shown in parentheses).*
2. *Cathode Indicator for SMS7621-079LF*
   Anode Indicator for SMS7630-079LF

200041-006

Figure 6. SC-79 Package Dimension Drawing



Notes:

1. *Carrier tape: black conductive polycarbonate or polystyrene.*
2. *Cover tape material: transparent conductive PSA.*
3. *Cover tape size: 5.4 mm width.*
4. *ESD-surface resistivity is ≤1 x 10^8 Ohms/square per EIA, JEDEC TNR Specification.*
5. *All measurements are in millimeters.*

200041-007

Figure 7. SC-79 Tape and Reel Dimensions

APPENDIX C

Laminate Specifications

NAN YA PLASTICS CORPORATION
ELECTRONIC MATERIALS DIVISION.
COPPER CLAD LAMINATE DEPARTMENT
NO. 201, TUNG HWA N. ROAD, TAIPEI, TAIWAN.

Issued: 2008/03/01
New: 2016/01/14

Glass cloth base epoxy resin
flame retardant copper clad laminate

NP-140TL

■ FEATURES

- Multi-functional epoxy renders the material outstanding heat resistance, better dimensional stability, and through-hole reliability that benefit the performance of high layer count multilayer boards.
- HTE copper foil applied to prevent corner cracking.
- High luminance of epoxy contrast with copper for laser type A.O.I.
- UV solder mask may be applied simultaneously in order to increase yields.
- IPC-4101D specification is applicable.

■ PERFORMANCE LIST

Characteristics	Unit	Conditioning	Typical Values	SPEC	Test Method
Volume resistivity	MΩ-cm	C-96/35/90	5.0×10^{6}	10^{5} ↑	2.5.17
Surface resistivity	MΩ	C-96/35/90	5.0×10^{7}	10^{4} ↑	2.5.17
Permittivity 1 MHZ	-	C-24/23/50	4.2-4.4	5.4 ↓	2.5.5.9
Permittivity 1 GHZ	-	C-24/23/50	3.8-4.0	-	2.5.5.9
Loss Tangent 1 MHZ	-	C-24/23/50	0.015-0.020	0.035 ↓	2.5.5.9
Loss Tangent 1 GHZ	-	C-24/23/50	0.012-0.014	-	2.5.5.9
Arc resistance	SEC	D-48/50+D-0.5/23	120 ↑	60 ↑	2.5.1
Dielectric breakdown	KV	D-48/50	60 ↑	40 ↑	2.5.6
Moisture absorption	%	D-24/23	0.20-0.30	0.35 ↓	2.6.2.1
Flammability	-	C-48/23/50	94V0	94V0	UL94
Peel strength 1 oz	lb/in	288℃x10" solder floating	10-14	6 ↑	2.4.8
Thermal stress	SEC	288℃ solder dipping	200 ↑	10 ↑	2.4.13.1
Glass transition temp	℃	DSC	140 ± 5	N/A	2.4.25
Dimensional stability X-Y axis	%	E 4/105	0.01-0.03	0.05 ↓	2.4.39
Coefficient of thermal expansion Z-axis before Tg Z-axis after Tg	 ppm/℃ ppm/℃	 TMA TMA	 50-70 250-350	N/A	2.4.24
Decomposition Temperature (Td 5% W/L)	℃	TGA	310	N/A	2.4.24.6

Data shown are nominal values for reference only.

NOTE:
The average value in the table refers to samples of .020" 1/1.
Test method per IPC-TM-650

Ordering Information
Contact your local sales representative or the Inside Sales Department in La Crosse, WI.

Phone: 1-800-845-2904 or
608-784-6070
Fax: 1-800-344-1825 or
608-791-2428

Isola Laminate Systems Corp.
230 North Front Street
La Crosse, WI 54601

For further information visit
www.isolalaminatesystems.com

ED130UV Typical Laminate Properties, 0.059" [1.5mm]

PROPERTY	UNITS	IPC 4101	ED130UV VALUE	CONDITIONING
Thickness	inches	1.5	0.059	—
	mm	[≥0.78]	[1.5]	—
Construction	—	—	8-7628	—
Retained Resin	%	—	44	—
Thermal				
Tg, min. (DSC)	°C	110	135	—
CTE - x-axis	ppm/°C	—	14	Ambient to Tg
y-axis	ppm/°C	—	13	Ambient to Tg
z-axis	ppm/°C	—	175	Ambient to 288°C
Solder Float, 288°C	seconds	—	>120	Condition A
Electrical				
Permittivity (DK), max. @				
1 MHZ	—	5.4	4.7	C-24/23/50
500 MHz	—	—	4.35	C-24/23/50
1 GHz (HP4291)	—	—	4.34	C-24/23/50
Loss Tangent (DF), max. @				
1 MHZ	—	0.035	0.020	C-24/23/50
500 MHz	—	—	0.017	C-24/23/50
1 GHz (2 Fluid Cell)	—	—	0.016	C-24/23/50
Surface Resistivity, min.	megohms	$1x10^4$	$2x10^5$	Condition F
	megohms	$1x10^3$	$1x10^8$	E-24/125
Volume Resistivity, min.	megohms-cm	$1x10^6$	$8x10^7$	Condition F
	megohm-cm	$1x10^3$	$2x10^7$	E-24/125
Dielectric Breakdown, min.	kV	40	55	D-48/50
Arc Resistance, min.	seconds	60	100	—
Comparative Tracking Index	PLC-UL	—	3	—
Physical				
Peel Strength, min. - 1 oz.	lb/in [Kg/M]	—	9.0 [161]	Condition A
		5.9 [105]	9.0 [161]	After Thermal Stress
		3.9 [70]	9.0 [161]	E-1/125
Flexural Strength, min.				
LW	psi [KG/M²]	60,000 [$4.23X10^7$]	80,000 [$5.63x10^7$]	Condition A —
CW	psi [KG/M²]	50,000 [$3.52X10^7$]	60,000 [$4.23X10^7$]	Condition A —
Warp & Twist	%	—	0.5	Condition A
Flammability	—	V-0	V-0	UL94
Moisture Absorption, max.	%	0.35	0.25	D-24/23
Tensile Strength				
LW	psi	—	50,000	Condition A
CW	psi	—	40,000	Condition A
Modulus of Elasticity				
Tensile Modulus (Young's)				
LW	psi	—	$3.5x10^6$	Condition A
CW	psi	—	$3.0x10^6$	Condition A
Flexural Modulus (Taylor's)				
LW	psi	—	$2.7x10^6$	Condition A
CW	psi	—	$2.4x10^6$	Condition A
Poisson's Ratio				
LW	—	—	0.136	Condition A
CW	—	—	0.118	Condition A

Data Sheet # 5020/3/01