Optimization of UHF voltage multiplier circuit for RFID application

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***Abstract*— This paper presents study and optimization of diode multiplier including antenna matching problems. Results on a voltage multiplier designed in 0.18μm CMOS process have been shown. It can powered a chip at a distance of 10 m with an efficiency of 30%. In this paper we present a simple analytical model of the complete tag: Antenna and chip. This model allows us to explain many results on crucial points of voltage multiplier design. We also present limitations of this kind of structure.**

I. Introduction

RFID (Radio frequency identification) system is constituted by a reader and a tag which must communicate together. The RFID tag is a transponder which consists in two parts: an antenna and a IC. It must recover power supply from the power derived from antenna. Actually a new demand appears on UHF RFID system which works around 915 MHz. Those new frequencies define in EPC specification [1] allow to work in a different way than system which operates at 13.56 MHz [2]. Indeed, the principle of inductive coupling is no more in use in this new system and so larger range can be reached. With new range the number of applications for RFID are always more important.

In the USA, the norm allows an emission power of 4 Watts, this value leads to a range around 10 m where the received power on the antenna is only 30μW. The converter must generate the DC voltage with the best efficiency possible in order to power the tag. The diagram on figure 1 presents an overview of the system. In the paper [3] a special attention is given to modulation, in this paper our principal goal is the supply generation and design optimization.

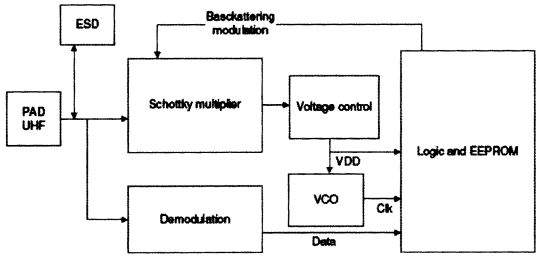

Fig. 1. Bloc diagram of the chip

The Converter or voltage multiplier is the most crucial element of transponders design and its power efficiency affects directly the performance of the system [3]. In this paper we choose the multiplier presented in figure 2. It is based on Schottky diodes which present low forward voltage and low substrate leakage. In section II we analyze the input of the transponder in order to give a simple model and estimate the input voltage and its dependence on impedance. We also explain how we proceed to find in simulation the input impedance of the chip and validate it with measure. In Section III, a method of optimization is given which take into account many extern parameters. An overview of problems which can affect directly efficiency of the system is given. Then, in section IV, results on an optimized multiplier are presented with impact on the power supply of frequency and range.

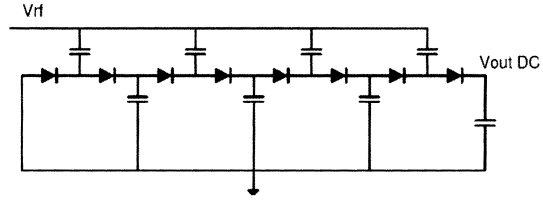

Fig. 2. Voltage multiplier which converts RF to DC

II. First approach

This kind of multiplier gives a DC voltage which depends on incident RF voltage. This transformation of voltage can be effective only if the input voltage is upper than Schottky forward voltage. In this study a special attention is payed to give a correct modeling of tag's input voltage. In this section, a model of the tag is presented in order to evaluate the quality factor at the input of the chip and so the input voltage. This simplified model leads us to the impedance problem. Indeed in order to have a correct idea of the input voltage, an accurate input impedance needs to be evaluate.

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A. Input Voltage dependance

The complete tag can be represented by its equivalent circuit which is constituted of a R,L for the antenna and R,C for the chip as shown in figure 3.

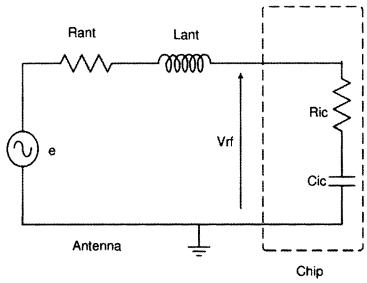

Fig. 3. Tag equivalent circuit

The f.e.m. provided by the antenna is given by equation 1

$$e = \sqrt{8 \times Rant \times P_r} \tag{1}$$

where P_r is the received power given by the Friss formula. The transfer function of the cell in figure 3 gives us the input voltage of the chip:

$$|Vrf| = \left| \frac{Zchip}{Zchip + Zant} \right| \times |e| \tag{2}$$

with $Zchip$ impedance of the chip and $Zant$ impedance of the antenna we can define:

$$Zant = Rant + j.Lant.\omega \tag{3}$$

$$Zchip = Ric + \frac{1}{j.Cic.\omega} \tag{4}$$

The figures 4 and 5 show the typical variation of Vrf for a chosen chip for different antenna. Those curves are valid for a range of 10 m.

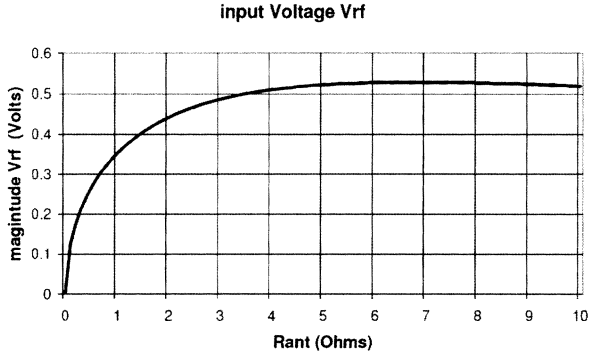

Fig. 4. Vrf for different Rant with Lant, Zchip fixed

Currently, in order to have a maximum power transfer between the antenna and the chip, the antenna have been designed to obtain condition of matching i.e. when $Zchip = Zant^*$. Under this condition Vrf is maximum, but a small variation of $Zant$ can rapidly decrease Vrf and lead to an insufficient input voltage. As an example, on figure 5 the magnitude of Vrf decrease from 0.53 V to 0.31 V for a variation of Lant of 10% in the same time the current across the Schottky is divided by 5. This places high constraints on imaginary part, whereas variation on real part have less impact on Vrf as shown in figure 4. Once the matching have been obtained, Vrf can be expressed with equation 2 taking into account that $Zchip = Zant^*$.

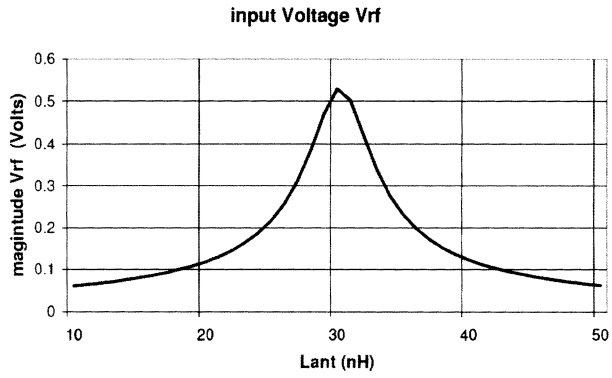

Fig. 5. Vrf for different Lant with Rant, Zchip fixed

$$|Vrf| = \left|\frac{e}{2}\right| \times \sqrt{1 + \left(\frac{1}{Ric.Cic.\omega}\right)^2} \tag{5}$$

In the case of our chip: $1 << \left(\frac{1}{Ric.Cic.\omega}\right)^2$ and with the equation 1:

$$|Vrf| = \frac{1}{Cic.\omega} \times \sqrt{\frac{2.Pr}{Ric}} \tag{6}$$

Equation 6 shows that it is possible to increase the input voltage of the chip with adapted impedance. Indeed decreasing Ric or Cic allows to get more important Vrf. However many limitations have to be mentioned:

- Decreasing Ric leads to reduce the chip consumption. (difficult for many operation such as writing in EEPROM)
- Increasing the quality factor reduce the band of frequency with Vrf upper than diodes forward voltage
- all antenna impedance are not realizable.

This results show the importance of input impedance of the chip which can improve the range of the system. Although adaptation is reached, the tag can not be powered if there is not a sufficient input voltage due to a weak quality factor.

B. Modelisation

Because of the sensitivity of the chip input, accurate values of impedance are needed. Therefore a previous work on impedance model of devices is necessary. Because of the

voltage multiplier topology (shown in figure 2) a special attention is given to Schottky and MIM capacitor. This work was performed in collaboration with ST Microelectronics. First Schottky have been designed and a DC model has been extracted thanks I-V measure at many temperatures. This model is then completed by a sub circuit which represents substrate leakage shown on figure 6. A test structure has been then designed, and RF measures of S parameters have permitted to extract values of substrate capacitor and resistor. The impedance of Schottky is then compliant with measure up to 10 GHz. Using a model which comes from RF measure permits to have correct current characteristic in the diode and also realist input impedance for the multiplier.

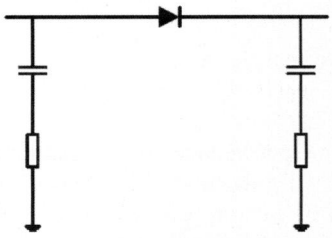

Fig. 6. extracted Schottky diodes

In the band of frequency use in this RFID, MIM capacitor have good quality factor. The most important parameter is the parasitic capacitors to the ground. Those capacitors are in parallel to diodes substrate's capacitor and their values have to be added.

C. Model validation

In simulation we use first harmonic impedance, which is, in this case, nonlinear function of power. As a consequence a power for adaptation must be chosen. Our choice is the minimum input power to attain the voltage needed by the chip. This power can be obtain by measurement or simulation. The figure 7 presents an example of measured variation of the tag voltage supply (Vdd).

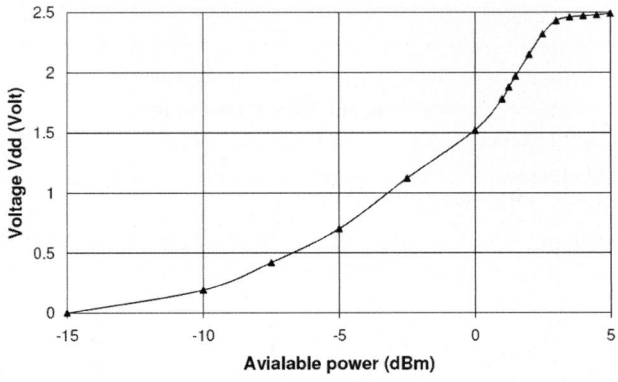

Fig. 7. Measured results of Vdd

In this example a power of -1.5 dBm is needed to obtain a Vdd of 1.2 V. This power is then use to find the input impedance. We use the ADS simulator with harmonic balance method. In all simulation the load of the voltage multiplier is calculated to be equal to 7 μA at 1.2 V.

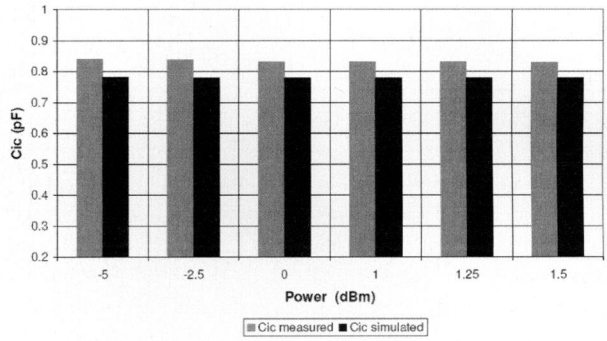

Fig. 8. Imaginary part of impedance at 915 MHz vs power

Figures 8 and 9 show the results of simulation of impedance in comparison to measured results. In those simulation, the source impedance is taken at 50 Ω to reproduce the source of the network analyser. A good correlation is obtained which permits to have correct input voltage in the multiplier. Then the simulation is in quasi real situation which take into account impedance mismatch between chip and antenna.

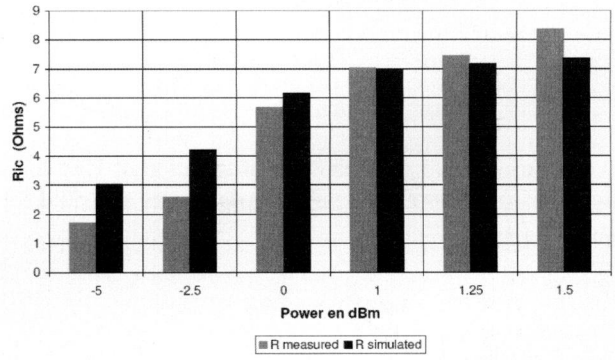

Fig. 9. Real part of impedance at 915 MHz vs power

III. VOLTAGE MULTIPLIER DESIGN

The optimization of this kind of multiplier must take many parameters into account. First of all, the need to have a voltage gain which allows the chip to be operational at long range. This parameter as explained before is dependent of input impedance. In a second time, the efficiency must be optimized to allow operations which need more consumption such as writing in the EEPROM. In order to obtain consistent results, in this paper, for each optimization of the circuit design many simulations must be done:

- the new impedance of the chip have to be found

- the antenna must be matched
- the simulation must be reloaded with this new parameters.

This method allows us to compare different designs of the multiplier. With this procedure the difference of results do not come from the adaptation mismatch. However, all impedance are not feasible for an antenna, that's why some results have to be ignored because their matching are impossible. The principal difficulty for antenna's impedance is to obtain small series resistance which must be equal to Ric.

A. Diodes Schottky

In a first time, it is necessary to make a choice about the Schottky diodes. In [4] and [5] design and layout of the Schottky are approached. The interest of interdigited diode has been shown. As explain in [3] there are two principal effects of diode design: a large surface of contact increases the current across the diodes and so system performance, on the other hand, large devices area increase substrates losses.
Some simulations have been done, and it appears that increasing the device and contact area is decreasing efficiency. That means that the current leaks in substrate, becomes more important than the current gain due to the contact area enlargement. Those results implicate that the diodes design is fixed by the capabilities of technologies: the diodes must be as small as possible with respect of design law and must get the largest number of contacts possible on this surface.

B. Number of stages

The figure 10 presents a variation of the number of multiplier's stages and its impact on the Vdd for a range of 10 m, for each result the input resistance of the chip is also given.

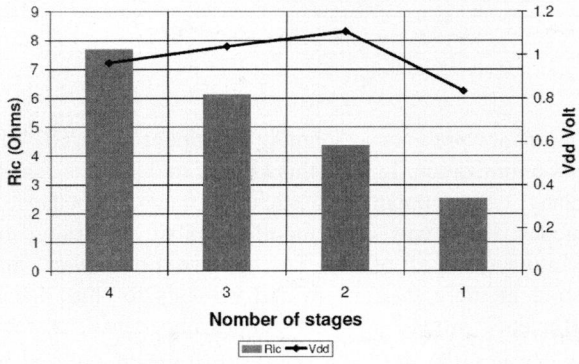

Fig. 10. Number of stage vs Voltage Vdd

This simulation takes into account the complete input of the chip with ESD, pad and demodulator. All theses elements consume power and reduce the final voltage Vdd reached.
With the figure 10 we deduce that the optimal solution for powered the tag is two stages. Indeed increasing the number of stages decreases, the voltage Vdd, two causes can explain this effect :

- with the multiplication of stages the area of the multiplier and the substrate's loss increases
- input resistance call for adaptation is small for low number of stages that involves an important Vrf in chip input (due to a large overvoltage)

C. Capacitors

An other parameter to optimize in multiplier design is the value of the capacitor. As shown in figure 2 there are two capacitors by stage. In consequence large value of capacitance leads to large area of circuit. However increasing capacitor can increase the power supply voltage as see on figure 11. The Vdd presented is obtained in 30μs.
The figure 11 also presents the variation of input resistance with those capacitors. The power supply reaches a maximum around 1.5 pF. Using larger capacitor leads to a small decreasing of Vdd due to a decrease of Vrf with Ric variation as shown in equation 6.

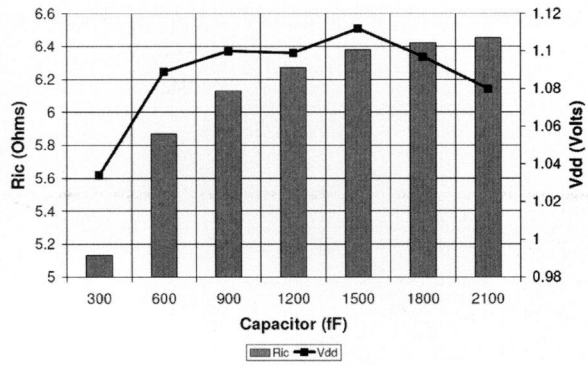

Fig. 11. Value of capacitor versus power supply vdd(30μs) and input resistance

Figures 10 and 11 present different optimizations for a multiplier in condition of adaptation. However this conditions are not always realizable: for example, it is difficult to design antenna with series resistance under 6 Ω. In consequence reducing the number of stages is not always possible. Increasing the capacitor can improve performance but the multiplier take too much place on the chip.
The capacitors used in the chip are MIM capacitors and present small parasitic capacitors to the ground, which are a crucial element for multiplier's performance. In each floating capacitor of multiplier, this small capacitor are in parallel with Schottky substrate capacitor. In our simulation a parasitic capacitor is taking into account. There are the sum of the two capacitors. In the simulation presented in figure 12 those parasitic capacitors have been modified in order to estimate the robustness of the circuit.

IV. Results

A multiplier has been designed alone in accordance to previous study. The number of stages is 3 because of antenna's constraints. The operating point is 1.2 V and 7μA. The

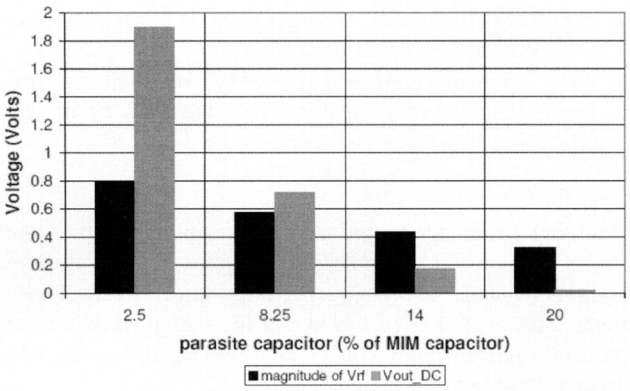

Fig. 12. effect of parasitic capacitor

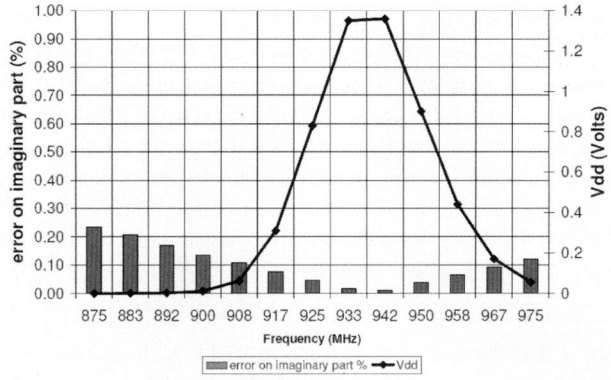

Fig. 14. Simulation Results

multiplier's capacitors are choose in order to get a chip area of 150μm x 180μm. In this condition the quality factor at chip input is around 30 when the operating point is reached. The results obtained have been presented in figures 13 and 14.

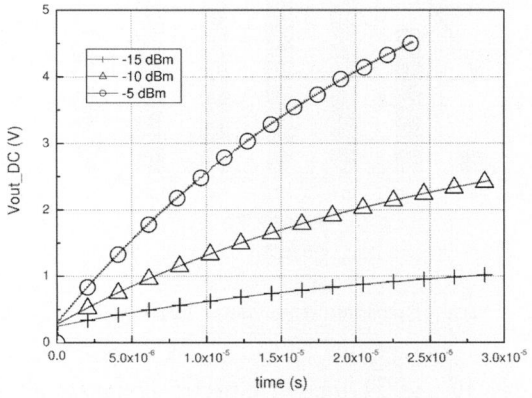

Fig. 13. Power supply Vdd for different avialable power

Figure 13 represents the power supply Vdd for different power, an available power of -15 dBm corresponds at a range of 10 m. At this distance a Vdd upper than 1 V can be obtained in 30 μs and more than 1.3 V in less than 100 μs. The antenna is modelized by a power source with an intern impedance: $Zant$. This impedance comes from Agilent MOMENTUM simulation of dipole antenna for each frequencies. The antenna has been designed to be adapted with the method presented in [6]. An error of less than 2 pourcent is reached at adaptation. The figure 14 shows us the frequency sensibility of this circuit for a distance of 10 m. The error between the imaginary part of antenna's impedance and the one necessary for adaptation is also presented. The multiplier is optimized for a narrow band of frequency compliant with the band 860 MHz-960 MHz of the EPC specification [1]. This band of frequency corresponds to an imaginary part well suitable.

An important parameter to increase range of different operations is efficiency. The table I presents for many available power the magnitude of Vrf, the power supply Vdd and the efficiency which is define as:

$$\eta = \frac{P_{DC}}{P_{RF}} \tag{7}$$

where P_{RF} is the input RF power and P_{DC} the DC power on Vdd.

TABLE I
EFFICIENCY VERSUS IMPUT POWER

Pin (dBm)	Vrf magnitude(Volts)	Vdd (Volt)	efficiency (%)
-16.3	0.74	1.32	32
-13.4	0.94	2.58	42
-10.6	1.20	3.29	50
-8	1.55	5.65	57
-5.4	2.00	8.02	64
-2.8	2.6	11.19	68

V. CONCLUSION

This paper presents a Schottky multiplier for UHF RFID and its optimization. Indeed, this kind of multiplier is sensitive at many extern parameters such as range, impedance or frequency, that's why each modification of the design must take into account all of this. The optimized multiplier can be powered at more than 10 m and presents for this distance an efficiency around 30 %. Its input impedance have been simulated in order to obtain value which can be realised with antenna design.

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