Modeling and Design of CMOS UHF Voltage Multiplier for RFID in an EEPROM Compatible Process

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***Abstract*—Modeling and design of CMOS ultra-high-frequency (UHF) voltage multipliers are presented. These circuits recover power from incident radio frequency (RF) signal and supply battery less UHF RF identification (RFID) transponders. An analytical model of CMOS UHF voltage multipliers is developed. It permits to determine the main design parameters in order to improve multiplier performance. The design of this kind of circuits is then greatly simplified and simulation time is reduced. Thanks to this model, a voltage multiplier is designed and implemented in a low-cost electrically erasable programmable read-only memory compatible CMOS process without Schottky diodes layers. Measurements results show communication ranges up to 5 m in the U.S. standard.**

***Index Terms*—MOSFET voltage multiplier, nonlinear model, passive transponders, radio frequency identification (RFID).**

I. Introduction

ULTRA-HIGH-FREQUENCY (UHF) radio frequency identification (RFID) applications increase rapidly [1]. The need for cheap tags for many applications imposes using low-cost CMOS process. In these applications, the integrated circuit (IC), is powered from the incident RF wave by means of an RF to the dc converter also named the voltage multiplier. In the U.S., the norm allows an emitted isotropic radiated power (EIRP) of 4 W, leading to a received power on the tag antenna that is only around 380 μW at 3 m which is the minimal communication range defined by the Electronic Product Code (EPC) specification [2]. Traditionally, voltage multipliers use a Dickson's charge pump [3] with Schottky diodes. These diodes allow low substrate losses and very fast switching. Unfortunately, they are often not available in standard electrically erasable programmable read-only memory (EEPROM) process and their use leads to a fabrication overhead. Moreover, the Schottky diodes forward voltage, which limits the RF-to-dc conversion efficiency, could not be easily decreased under 0.3 V in silicon process because of Schottky barrier height [4], [5]. On the other hand, natural MOS transistors are often available. They have a threshold voltage (vt) which can be decreased around 0.1 V. With special care to minimize RF substrate losses and the parasitic capacitance, which are an important penalty for the RF-to-dc conversion efficiency, the use of natural MOS transistors in RFID voltage multipliers is an interesting alternative in order to reduce the fabrication cost [6].

Previous studies give a model for this kind of multiplier [7], [8], but the new model presented in Section II, allows taking into account both MOS nonlinearity and RF losses. In addition, this model determines analytically chip input voltage $V_{\rm rf}$ and input impedance, which is an important parameter for matching the antenna. Then, impact of important design parameters can be investigated. The design of such low-cost RF-to-dc converter without using Schottky diodes is optimized in Section III, thanks to the model. Section IV presents results on a voltage multiplier implemented in a low-cost EEPROM compatible CMOS process. Measurement results show communication ranges capabilities up to 5 m in the U.S. standard.

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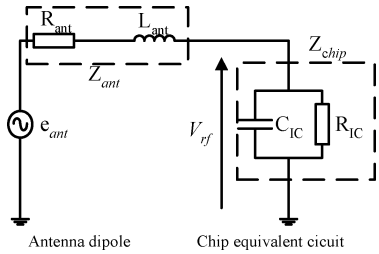

Fig. 1. Antenna and chip equivalent representation.

II. Voltage Multiplier Modeling

The input impedance of an UHF RFID IC is capacitive [9]. An antenna with inductive output impedance is generally used to achieve a power matching [10]. The equivalent circuit including the antenna and the tag input at the fundamental frequency of the incident RF wave is given in Fig. 1. The input impedance (Zchip) of the chip is composed of $R_{\rm IC}$ and $C_{\rm IC}$, which are nonlinear functions of the magnitude of the input voltage V_Rf. $R_{\rm IC}$ represents the voltage multiplier losses and the useful dc current available at multiplier output. $C_{\rm IC}$ varies both with the number of multiplier stages, active device's sizes and includes pad and electrostatic discharge (ESD) equivalent capacitors. The Friis formula permits to determine the voltage $e_{\rm ant}$ provided by the antenna

$$e_{\rm ant} = \sqrt{8 \times {\rm Re}\,(Z_{\rm ant}) \times P_R} \tag{1}$$

where P_R is the available power at the antenna output $Z_{\rm ant}$ the antenna's impedance. Under power matching, both the input

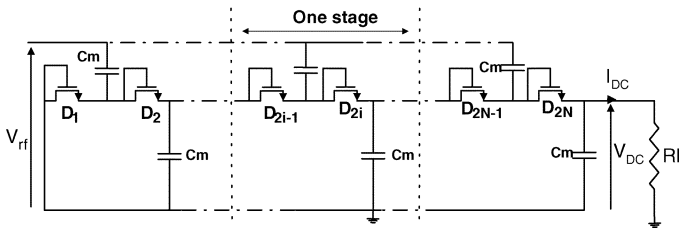

Fig. 2. N-stage voltage multiplier.

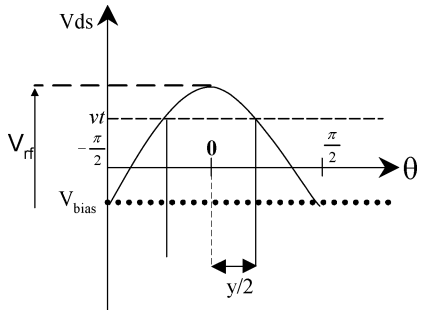

Fig. 3. MOSFETs bias versus angle.

voltage $V_{\rm rf}$ magnitude and the IC input power are maximum. The maximum input voltage magnitude is given by

$$|V_{\rm rf}|_{\max} = \sqrt{2 \times \mathrm{Re}\,(Z_{\rm chip}) \times P_R \times (1 + Q_{\rm IC}^2)} \qquad (2)$$

where $Q_{\rm IC}$ is the IC quality factor.

In charge pumps, the output dc voltage ($V_{\rm dc}$) increases with the input voltage magnitude. Consequently, an increase of the IC Q factor allows an extended communication range for the same radiated power.

In order to optimize the voltage multiplier design an analytical model is developed in the next subsections. With a few MOSFET parameters, this model allows computing the incident voltage $|V_{\rm rf}|$ that achieves a desired dc current at the multiplier output. The calculated $|V_{\rm rf}|$ is a function of the number of multiplier stages (N) and the MOSFET's sizes W and L. This model also gives the input impedance of the multiplier and consequently, the communication range under power matching conditions by using Friis formula.

A. Magnitude of Incident Voltage Calculation

1) Analytical Modelization: An N-stage voltage multiplier circuit is shown in Fig. 2. In a CMOS voltage multiplier, the diodes are synthesized by MOS transistors. Considering that the multiplier's capacitors C_m act as dc blocks, the dc current flows from the ground to the load through each diode. If the diodes D_I are identical, their dc bias is

$$V_{\rm bias} = -\frac{V_{\rm dc}}{2N}. \qquad (3)$$

On the other hand, for the incident RF wave the capacitors C_m act as short circuits. Consequently, the sinusoidal RF incident voltage is applied to every diode D_I. Each MOSFET is driven as in class C amplifiers as shown in Fig. 3 with a conduction angle y given by

$$y = 2 \cdot \arccos(x) \qquad \text{with} \quad x = \frac{vt - V_{\rm bias}}{|V_{\rm rf}|}. \qquad (4)$$

If we assume that $I_{\rm ds} \approx 0$ when $V_{\rm gs} < vt$ and that the drain current $I_{\rm ds}$ follows a quadratic current law elsewhere, the expression of the current across each transistor during the conduction time is

$$I_{\rm ds} \approx \mu \cdot C_{\rm ox} \cdot \frac{W}{2L} \cdot (V_{\rm gs} - vt)^2 \quad \text{if} \quad V_{\rm gs} > vt. \qquad (5)$$

This quadratic law is used here because, usually, natural MOS are available only for length larger than a minimal value around 1 μm. In addition, in order to get a straightforward model, bulk effect is not considered in (5).

Current calculation in class C has been developed in [11] with a linear current law. With quadratic law, current equation can be expressed with conduction angle

$$I_{\rm ds}(\theta) = I_{\rm ds\,max} \left[\frac{\cos(\theta) - \cos\left(\frac{y}{2}\right)}{1 - \cos\left(\frac{y}{2}\right)} \right]^2. \qquad (6)$$

This equation can be expended in a Fourier series, the dc current $I_{\rm dc}$, and the fundamental of the drain current I_{d1} can be calculated by

$$I_{\rm dc} = \frac{1}{2\pi} \int_{-y/2}^{y/2} I_{\rm ds}(\theta) d\theta \qquad (7)$$

$$I_{d1} = \frac{1}{\pi} \int_{-y/2}^{y/2} I_{\rm ds}(\theta) \cos(\theta)\, d\theta. \qquad (8)$$

Solving (7) with (6) and (4) yields an analytical expression for $I_{\rm dc}$

$$I_{\rm dc} = \frac{Kd \cdot W \cdot |V_{\rm rf}|^2}{4 \cdot \pi \cdot L} \cdot \left[\arccos(x) \cdot (1 + 2x^2) - 3 \cdot x \cdot \sqrt{1 - x^2} \right] \qquad (9)$$

with $Kd = \mu \cdot C_{\rm ox}$.

This equation can be solved numerically to get the value of $|V_{\rm rf}|$ with fixed $I_{\rm dc}$ and $V_{\rm dc}$. With this calculated $|V_{\rm rf}|$, it is possible to determine I_{d1} with (8)

$$I_{d1} = \frac{Kd \cdot W \cdot |V_{\rm rf}|^2}{4 \cdot \pi \cdot L} \cdot \left[\sqrt{1 - x^2} \cdot \left(\frac{2}{3} \cdot x^2 + \frac{4}{3} \right) - 2 \cdot x \cdot \arccos(x) \right] \qquad (10)$$

impact of important design parameters (N, W, L) are then brought out.

2) Validation: The analytical model and the simulation results with a MM9 models from Design kit are compared for different bias.In simulation, the operating point is fixed by $V_{\rm dc}$ and the load resistor (Rl). Fig. 4 shows the comparison for many multipliers operating points for a 0.18-μm CMOS proces

The analytical model gives values of $|V_{\rm rf}|$ compliant with design kit simulation. For $V_{\rm dc}$ upper than 2.5 V, a small difference is observed which can be decreased by considering the bulk effect on the model. However, in this kind of circuit, the maximum

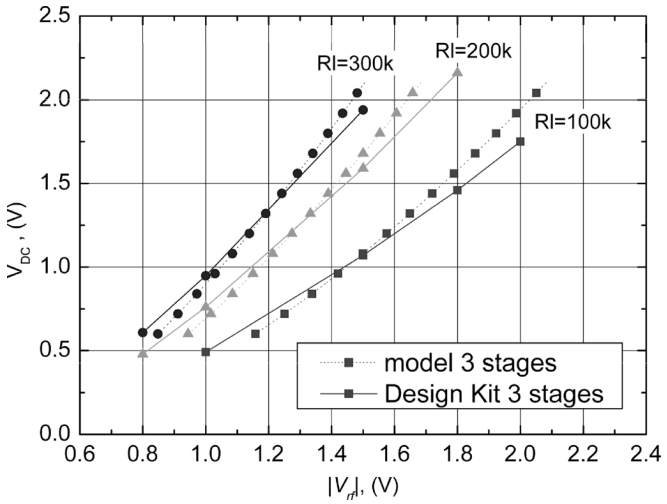

Fig. 4. $|V_{\rm rf}|$ needed to obtain fixed VDC.

dc supply is close to 1.8 V and considering bulk effect is not necessary.

Without the analytical model, as $|V_{\rm rf}|$ is not known *a priori*, it is difficult to get a simulation point with desired output values $V_{\rm dc}$ and $I_{\rm dc}$. Consequently, much iteration must be done. Each of iterations corresponds to a time-domain simulation with a time step smaller than the RF period. The final time needed to charge the largest capacitor is generally around 30 μs for a RF period around 1 ns. Another issue is to use harmonic balance or envelope simulation, which are faster. However, in order to optimize multiplier and determine best designs parameters many simulations are needed.

Consequently, an analytical model is very helpful. Indeed, it allows studying influence of the design parameters of the voltage multiplier N, W, and L, on the multiplier electrical performances and characteristics: power efficiency and input impedance. A systematic study with a design kit and time-domain simulations will consume a huge simulation time.

B. IC Impedance Calculation

1) Analytical Modelization: Assuming that the multiplier's capacitors C_m have large enough value to be considered as short circuits for the RF voltage, the IC impedance is formed by the $2N$ MOSFETs in parallel, also in parallel with pads and ESD.

In order to compute the MOSFETs impedance, the fundamental of the drain current I_{d1} is calculated (10). Then the nonlinear resistive part of each of MOSFETs impedance at first harmonic can be computed for a given $V_{\rm rf}$ input voltage magnitude

$$R_{\rm mos} = \frac{|V_{\rm rf}|}{|I_{d1}|}. \tag{11}$$

Considering the multiplier topology for each stages (Fig. 2), and if the impedance of the capacitors C_m is large enough to be negligible around 900 MHz, each impedance stage can be calculated with the equivalent circuit given on Fig. 5. On this circuit, substrate losses are taken into account by the network Rs, Cs. For one MOSFET size, Rs and Cs values are extracted

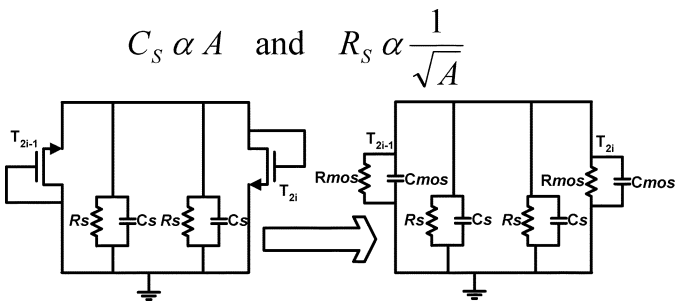

Fig. 5. One-multiplier-stage equivalent circuit.

from S parameters measurements on a test structure. Impact of area (A) is then considered with (12) [12]

$$C_S \alpha A \quad \text{and} \quad R_S \alpha \frac{1}{\sqrt{A}}. \tag{12}$$

Substrate losses are in parallel with the MOSFET equivalent circuit $R_{\rm mos}\, C_{\rm mos}$. The complete chip input impedance including the input pads and the ESD protection circuit is given in (13) and (14). ESD and pads effects are negligible on the resistive part of the IC impedance. However, they must be taken into account on the imaginary part of the input impedance

$$R_{\rm IC} = \frac{1}{2N} \frac{R_{\rm mos} R_S}{R_{\rm mos} + R_S} \tag{13}$$

$$C_{\rm IC} = 2N\,(C_{\rm mos} + C_S) + C_{\rm pad} + C_{\rm ESD}, \quad \text{with} \quad C_{\rm mos} = C_{\rm ds} + C_{\rm gs}. \tag{14}$$

The capacitor issue from multiplier design which can be expressed by $2N \cdot (C_{\rm mos} + C_s)$ is around a few tens of feratofarads. This small value is insignificant versus ESD and pad value, which are around 400 fF. With this consideration, $C_{\rm IC}$ can be expressed as

$$C_{\rm IC} \approx C_{\rm pad} + C_{\rm ESD}. \tag{15}$$

Thanks to this model, we can determine the first harmonic impedance of the chip and optimize it in order to get sufficient input voltage in order to reach a fixed operating point ($V_{\rm dc}$, $I_{\rm dc}$).

2) Validation: Design kit simulation of $R_{\rm IC}$ and its analytical model are compared on Fig. 6. Moreover, these results show the impact of operating point and number of stages on the input resistance. Each of operating point corresponds to an output power also presented on the Fig. 6.

A good agreement is observed for different number of multiplier stages and operating point.

C. Power and Efficiency Calculation

All the previous model results allow calculating two important design parameters.

The input power of the chip in the case of perfect matching

$$P_{\rm in} = \frac{|V_{\rm rf}|}{2 \cdot R_{\rm IC}} \tag{16}$$

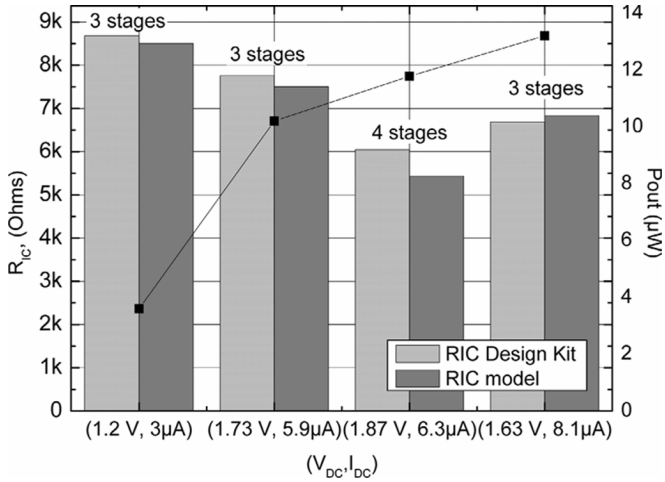

Fig. 6. $R_{\rm IC}$ for different design.

and the efficiency

$$\text{Efficiency} = \frac{P_{\rm out}}{P_{\rm in}} \quad \text{with} \quad P_{\rm out} = V_{\rm dc} \cdot I_{\rm dc}. \qquad (17)$$

With little information about the transistors, the analytical model leads us to the main multiplier characteristics. The determination of a needed input power for a fixed operating point is very helpful information in order to evaluate the communication range.

III. Design

Without an analytical model the design of this kind of circuit needs a lot of simulations. Indeed, much iteration are needed to find a functional multiplier, moreover designer do not know if his design is optimal. In this section, each design parameter is discussed in order to find most advantageous multiplier performance.

A. W and L Parameters

Thanks to the previous model, transistors sizes for optimal result can be computed. For a fixed operating point, the model gives $|V_{\rm rf}|$ and $R_{\rm IC}$, so we can determine the input power versus transistors sizes (W, L).

The best choice for this kind of circuit is a device that allows reaching a desired operating point for a minimum input power. Fig. 7 shows that L must be minimum to get $P_{\rm in}$ minimum, whereas there is an optimal size for W around 0.4 μm in this technology.

B. Number of Stages

Table I gives the minimum power needed for an operating point of 1.2 or 1.7 V at 3 μA. The number of stages affects greatly the input impedance. Consequently, if the minimum input power for a fixed operating point is the best choice in terms of IC design, the designer must pay attention to antenna matching possibility.

According to the analytical model, a one-stage multiplier can not reach 1.7 V at 3 μA . This result implies that a one-stage multiplier cannot be used in RFID system where voltage at multiplier output is more important than regulated voltage around 1.2 V. The model allows tracing multiplier's efficiency versus transistor size and number of stages. Fig. 8 shows the results for $I_{\rm dc} = 3$ μA and transistor length set to the minimal value according to previous results.

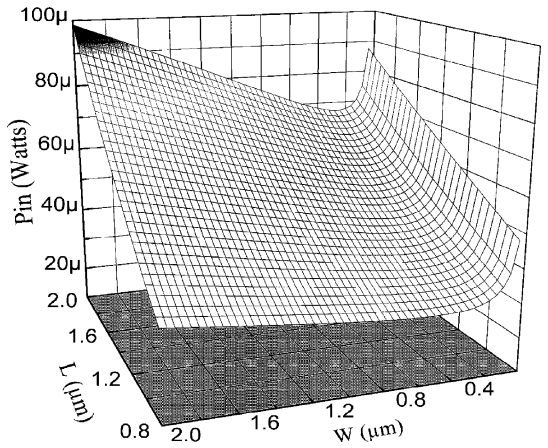

Fig. 7. Input power versus transistors sizes for a three-stage multiplier with $P_{\rm out} = 1.2$ V $\cdot$ 3 μA.

TABLE I
$P_{\rm in}$ VERSUS NUMBER OF STAGES

Number of Stages	1	2	3	4	5
P_{in} (µW) Needed for 1.2V	40.89	52.4	65.7	79.61	93.7
P_{in} (µW) Needed for 1.7V	-	63.9	76.35	89.73	103.5

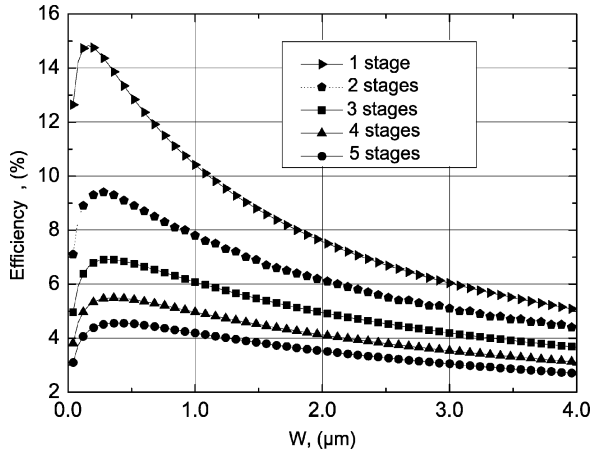

Fig. 8. Multiplier efficiency for different number of stages and $I_{\rm dc} = 3$ μA.

One and two-stage multiplier needs a high-Q antenna, which is not easily feasible in low-cost material. So a multiplier with three stages presents the minimum input power (Table I) with feasible input impedance (resistance 8 kΩ and capacitance around 600 fF). At optimal efficiency, W and the fixed number of stages can be found

IV. Results

A test chip has been realized (Fig. 9). The multiplier implemented in 0.18-μm CMOS process is a three-stage multiplier with C_m of 1.2 pF and $Vt = 0.28$ V. The multiplier's area is

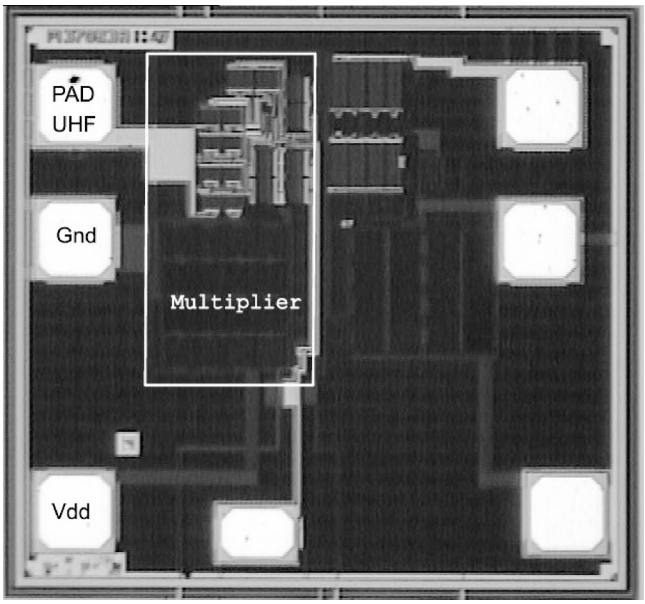

Fig. 9. Chip photography.

TABLE II
ON WAFER MEASUREMENT AND ANALYTICAL RESULTS FOR 3 μA AT 1.2 V

	modeled	Measured	Simulated
R_{IC}	8.5KΩ	10 KΩ	8.666 KΩ
Cic	503 fF	579 fF	509 fF
Efficiency	5.5 %	6.3%	5.3%

180 μm$\times$ 90 μm. The transistors size are set to the minimum value allowed in the technology. This chip integrates the multiplier and the ESD protection circuit. A large capacitor of 200 pF is used at the dc output to stock the power. A resistive load is connected to the multiplier output in order to emulate the IC consumption, which is about 3 μA at 1.2 V. This consumption was measured on a working tag in the same technology.

On wafer measurements with a network analyzer allow verifying circuit impedance and functionalities. Results at the operating point are given in Table II, they validate the design and the simulation. In order to determine the correct $P_{\rm in}$, impedance measurement is also done. The input power $P_{\rm in}$ is then calculated taking into account the mismatch between the chip and the network analyzer.

In a second time, range measurement is done with the chip bonded to an antenna. Special care is taken with antenna matching in order to minimize losses between chip and antenna [13]. The measured voltage VDC provided by the multiplier is shown on Fig. 10 for an EIRP of 4 W, analytical model results are. The antenna of the measured tag is around 1 dB, but model does not take into account interconnection between chip and antenna. In the same 0.18-μm CMOS process, the tag needs 1.2 V to be powered. This voltage can be achieved with this voltage multiplier for communication range up to 5 m. On the same technology, a multiplier with Schottky diodes gets a communication range of 7.5 m [5], but fabrication process is more expensive because of an increase of number of mask.

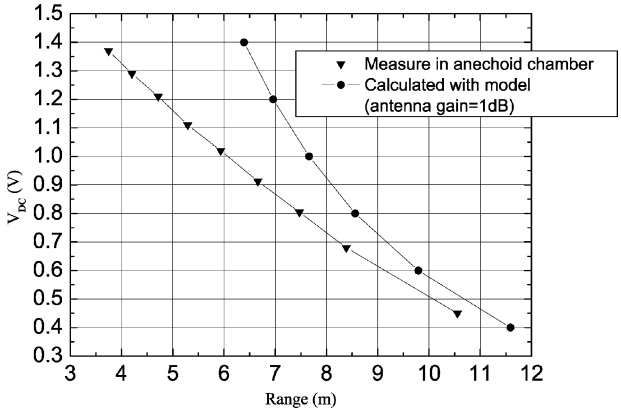

Fig. 10. $V_{\rm dc}$ versus range measurement.

V. CONCLUSION

An analytical model of MOSFET voltage multipliers is presented. Simulations with design kit and measurements are compliant with this model. It allows with a few input parameters and with short calculation time to design an optimal multiplier. A multiplier implemented in a fully compatible EEPROM CMOS process show capability to supply a RFID chip from 0 to 5 m. The theory and experiment have demonstrated the ability to make a fully CMOS voltage multiplier.

REFERENCES

[1] K. Finkenzeller, *RFID Hanbook*. New York: Wiley, 1998.
[2] *EPC, Specification for RFID Air Interface*. Bristol, U.K.: EPCglobal, 2004.
[3] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power," *IEEE J. Solid State Circuits*, vol. 38, no. 9, pp. 1602–1608, Sep. 2003.
[4] F. Roccaforte, F. La Via, S. D. Franco, and V. Raineri, "Dual metal SiC Schottky rectifiers with low power dissipation," *Microelectron. Eng.*, vol. 70, pp. 524–8, 2003.
[5] E. Bergeret, J. Gaubert, P. Pannier, and J. M. Gaultier, "Conception of UHF voltage multiplier for RFID circuit," in *Proc. North-East Workshop Circuits Syst.*, Jun. 2006, pp. 217–220.
[6] C. Y. Bun and Y. W. Gan, "Air-interfacing microwave passive RFID tag in bulk CMOS," in *Proc. 2005 IEEE Int. Workshop Radio Freq. Integr. Technol.*, Singapore, Dec. 2, 2005, pp. 65–69.
[7] J. P. Curty, N. Joehl, F. Krummenacher, C. Dehollain, and M. J. Declercq, "A model for μ-power rectifier analysis and design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2771–2779, Dec. 2005.
[8] J. Yi, W.-H. Ki, and C.-Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 1, pp. 153–166, Jan. 2007.
[9] G. De Vita and G. Iannaccone, "Design criteria for the RF section of UHF and microwave passive RFID transponders," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2978–2990, Sep. 2005.
[10] P. V. Nikitin, K. V. S. Rao, S. F. Lam, V. Pillai, R. Martinez, and H. Heinrich, "Power reflection coefficient analysis for complex impedances in RFID tag design," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 8, pp. 2721–2725, Aug. 2005.
[11] R. Gupta, B. M. Ballweber, and D. J. Allstot, "Design and optimization of CMOS RF power amplifiers," *IEEE J. Solid- State Circuit*, vol. 36, no. 2, pp. 166–175, Feb. 2001.
[12] C. Enz, "MOS transistor modeling for RF IC design," in *Proc. GAAS'00*, Paris, France, Oct. 23, 2000.
[13] K. V. S. Rao, P. V. Nikitin, and S. F. Lam, "Antenna design for UHF RFID tags: A review and a practical application," *IEEE Trans. Antennas Propag.*, vol. 53, no. 12, pp. 3870–3876, Dec. 2005.