Variable Frequency AC Source

Project Proposal

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Project Summary:
The goal of this senior project is to design, build, and test a variable frequency AC source (VFACS). The VFACS shall be designed as a single-phase AC source for input signal frequencies between 0 and 60 Hz. If time permits, the system will be modified to provide a three-phase AC source intended to operate a three-phase induction motor for input signal frequencies between 0 and 60 Hz. The system shall be capable of operating at 208 V_{rms} while supplying 5 A_{rms} per (implemented) phase.

Project Description:
The VFACS shall be composed of 5 subsystems as follows:

- PWM Generation Controller
- Gate Drive Circuitry
- Inverter
- Filter
- Load

A high level system block diagram of the VFACS system is shown below in figure 1. Each component of the system shall be developed and tested sequentially. When the testing of one subsystem is complete and the performance is satisfactory, the next subsystems will be built and tested. The interconnections and inputs of the VFACS system are listed in table 1.

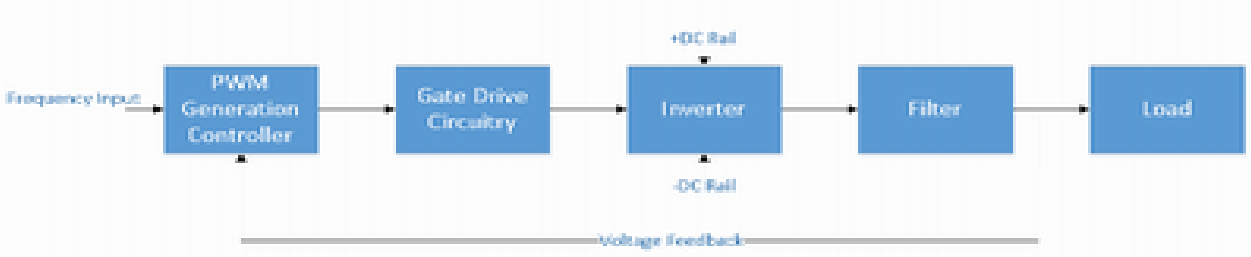

Figure 1: High Level System Block Diagram

VFACS Subsystem Connection Lists					
	Subsystem	**# of Inputs**	**Subsystem Input Source**	**# of Outputs**	**Subsystem Output Target**
1	PWM Generation Controller	2 (single phase) 4 (three-phase)	Frequency Input Load Voltage Feedback[1]	2 (single phase) 6 (three-phase)	Gate Drive Circuitry
2	Gate Drive Circuitry	2 (single phase) 6 (three-phase)	PWM Gen. Controller	2 (single phase) 6 (three-phase)	Inverter
3	Inverter	2 (single phase) 6 (three-phase)	Gate Drive Circuitry	1 (single phase) 3 (three-phase)	Filter
4	Filter	1 (single phase) 3 (three-phase)	Inverter	1 (single phase 3 (three-phase)	Load
5	Load	1 (single phase) 3 (three-phase)	Filter	1 (single phase) 3 (three-phase)	Load Voltage Feedback*

*Feedback to the PWM Generation Controller will be measured at load terminals using a Nat. Instru. cDAQ

Table 1: VFACS Sub System Connection (I/O) List

PWM Generation Controller:

This subsystem shall produce the appropriate PWM signal to represent the desired sine wave selected by the user. The PWM output signal provided by this subsystem will be the input to the Gate Drive Circuitry portion of the system. Time permitting; the PWM for the three-phase system shall also use this module to produce the required sine waves. The block diagram used to produce this component can be seen in figure 2. A Simulink model for the V/Hz controller is shown in figure 4, with a graph in figure 5.

[1] These components may change based on performance during testing

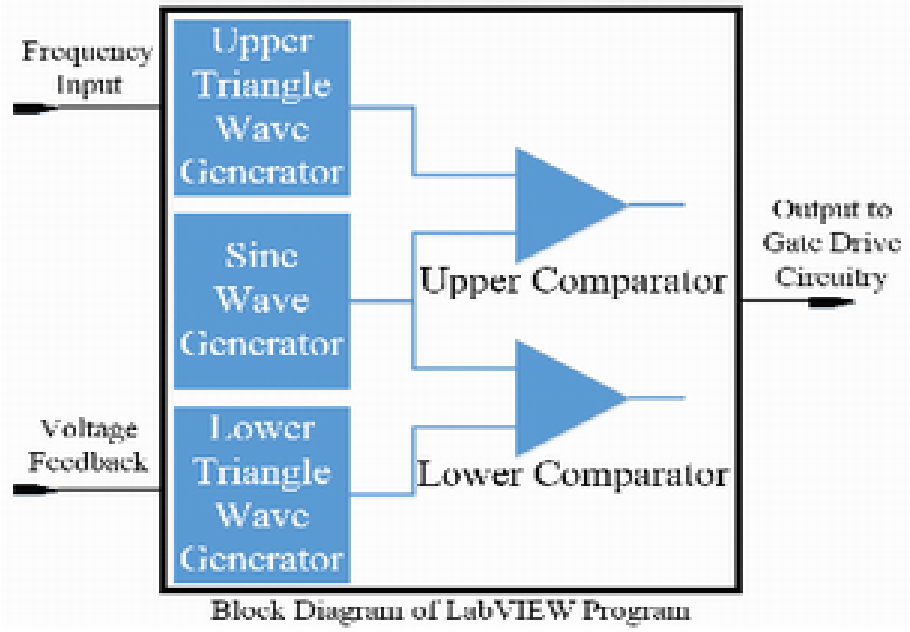

Figure 2: Overall System Block Diagram for LabVIEW Program

The signal produced by the PWM generation controller shall:

- Be generated based on the user's frequency input and voltage feedback from the load
- Be produced using a LabVIEW based cDAQ controller from National Instruments
- Be produced by comparing a sine wave and two triangle waves as shown in figure 3
- Use two 15 KHz triangle waves and a variable amplitude sinusoid with 0-60 Hz frequency
- Produce a constant V/Hz ratio based on the input voltage, with a ratio of 0.5892 for initial 35 V_{rms} testing and a ratio of 3.467 for the 208 V_{rms} system (again, if time permits).

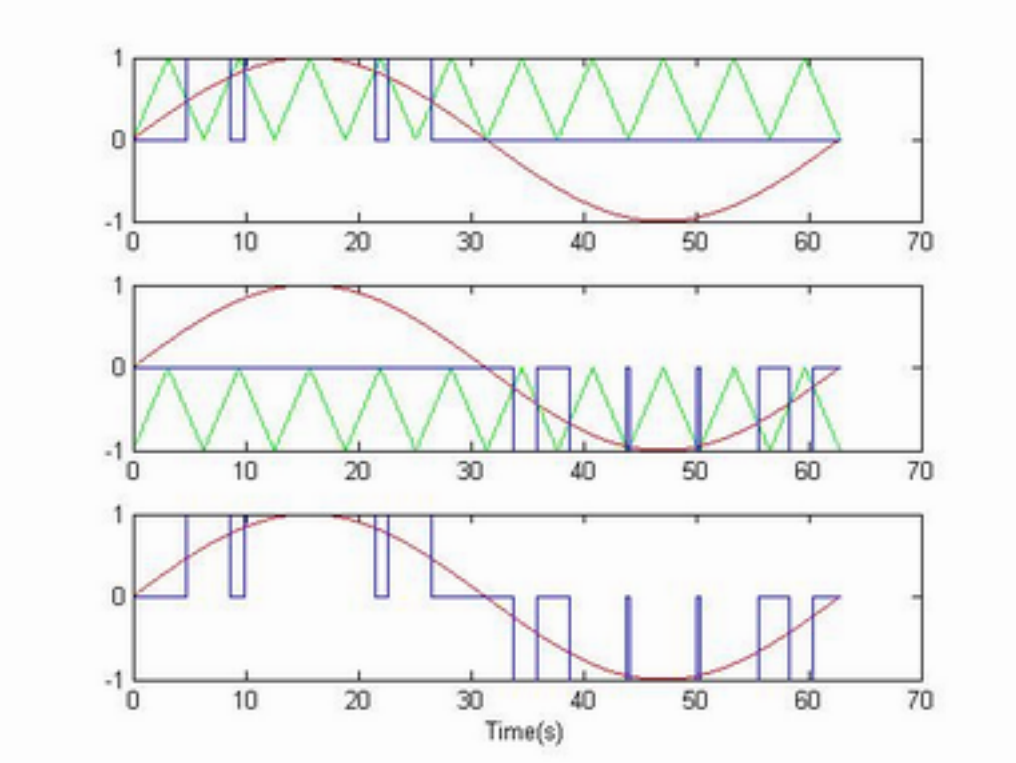

Figure 3: Examples of Sine, Triangle, and PWM Waveforms

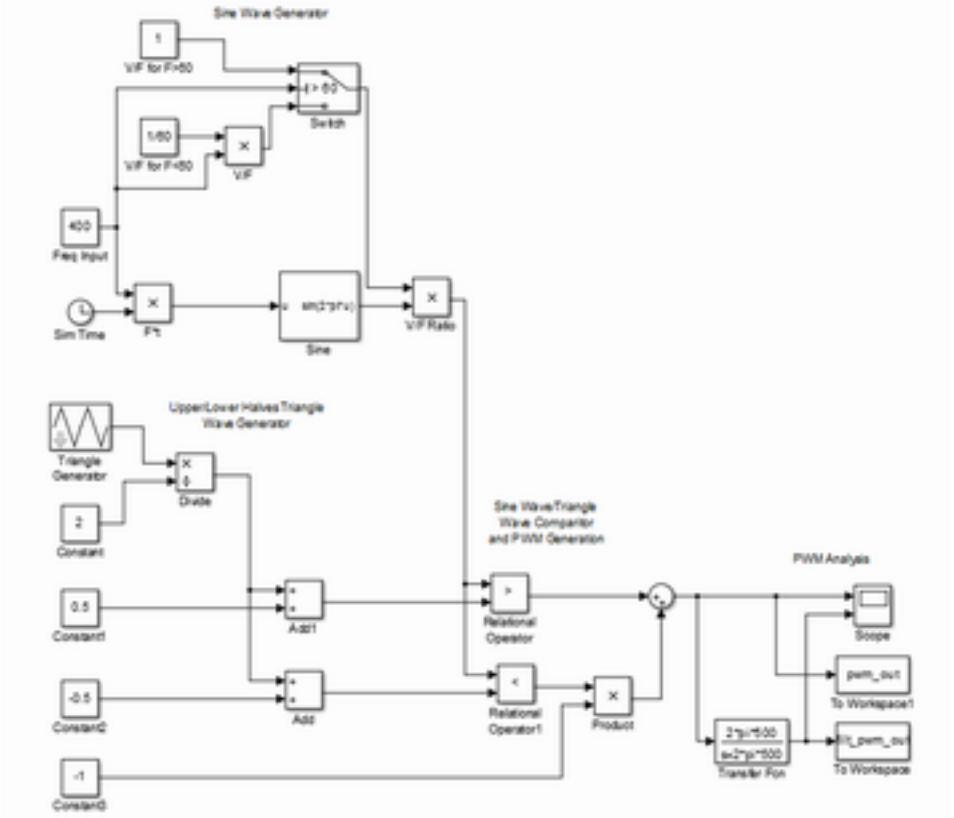

Figure 4: Simulink model of V/Hz ratio controller

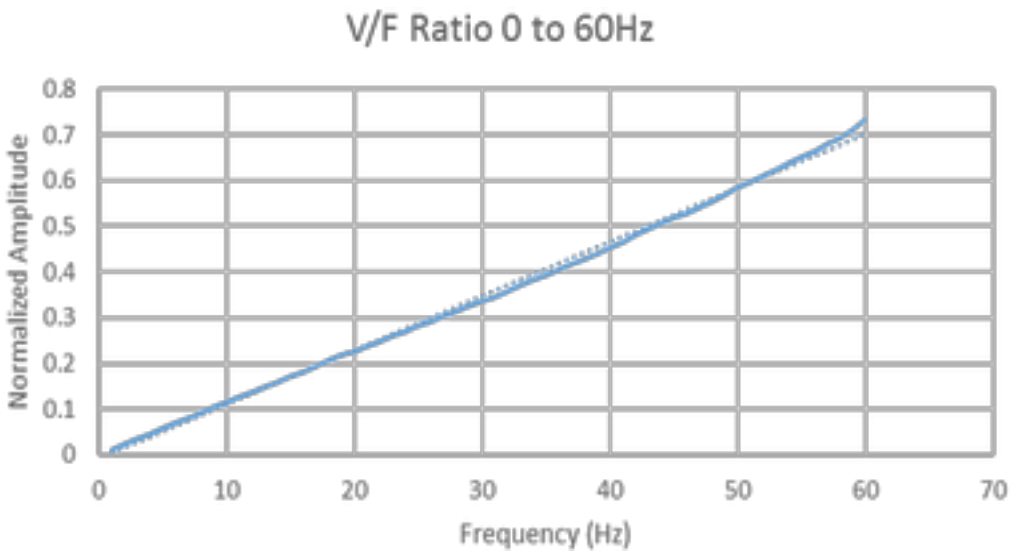

Figure 5: Plot showing constant V/Hz ratio

Gate Drive Circuitry:

In the VFACS system, the gate drive circuitry will be used to protect the inputs of the cDAQ controller from voltage spikes inherent in switching inductive systems as well as to amplify the TTL level signal from the PWM Generation Controller to the 0-15 V level required to drive the IGBTs in the Inverter. This will be accomplished by using a high speed optical isolator and gate driver. Components will be selected based on robustness and availability. The preliminary gate drive circuit is shown in figure 6.

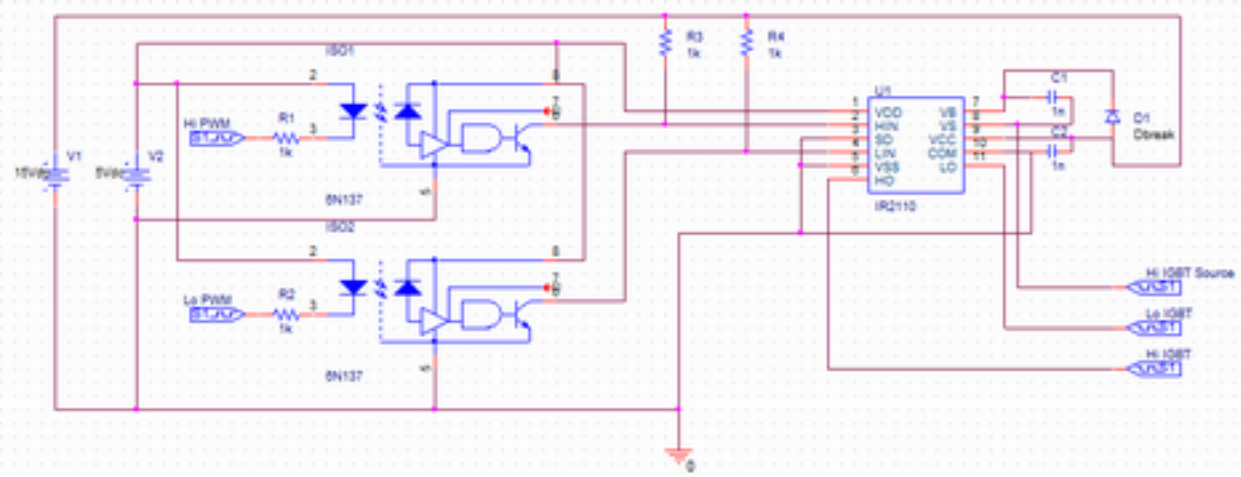

Figure 6: Gate drive circuit schematic

The gate drive circuitry must be capable of switching at 1% duty cycle at a15 [kHz] switching frequency without clipping. The 6N137 optical isolator will isolate the CDAQ outputs from the inverter, filter, and load. The IR2110 gate driver will amplify the PWM signal from TTL voltage and current levels to the +15 [V] and 2[A] required to drive the inverter. The IR2110 gate driver will drive both high and low sides of the H-bridge IGBT's from a single chip.

Inverter:
The inverter shall be used to amplify the PWM signal produced by the PWM Generation Controller to a usable level for an AC machine. It shall use IGBT pairs with anti-parallel diodes and a DC power supply to accomplish this goal. IGBTs were chosen for their high voltage capabilities and availability. The first design iteration of the inverter shall be for a single phase configuration as shown in figure 7, and the second design iteration shall be for a three-phase configuration as seen in figure 8 (if time permits). The DC rails used in the inverter will utilize 0 and 100 V for the testing phase. In the final step of the project, a source conversion shall be performed to eliminate a DC power supply and use three-phase AC power to generate the DC rails (this step will be completed only if sufficient time remains in the semester).

The incoming PWM signal from the gate drive circuitry shall be encoded in two separate signals, an upper half PWM and lower half PWM. The upper half PWM shall drive the upper IGBT and the lower half PWM signal shall drive the lower IGBT. The IGBT configuration and the timing of the upper and lower half PWM signals shall combine the two, single sided PWM signals into one dual sided PWM signal. This will represent the sinusoidal wave necessary to drive a single-phase AC load.

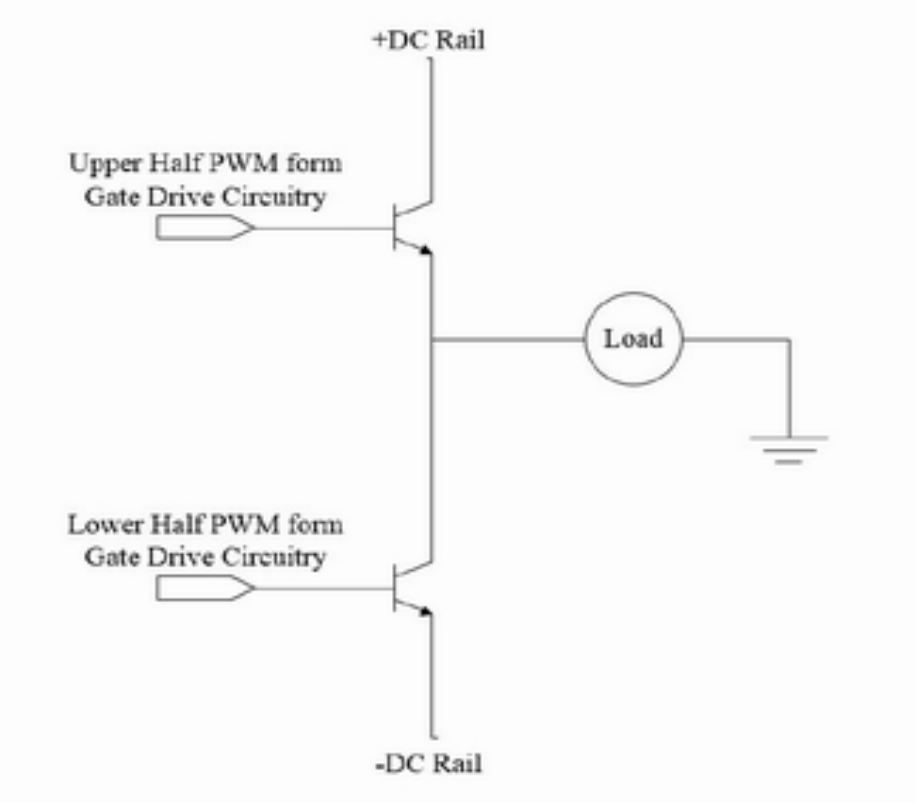

Figure 7: Single-Phase Inverter Configuration

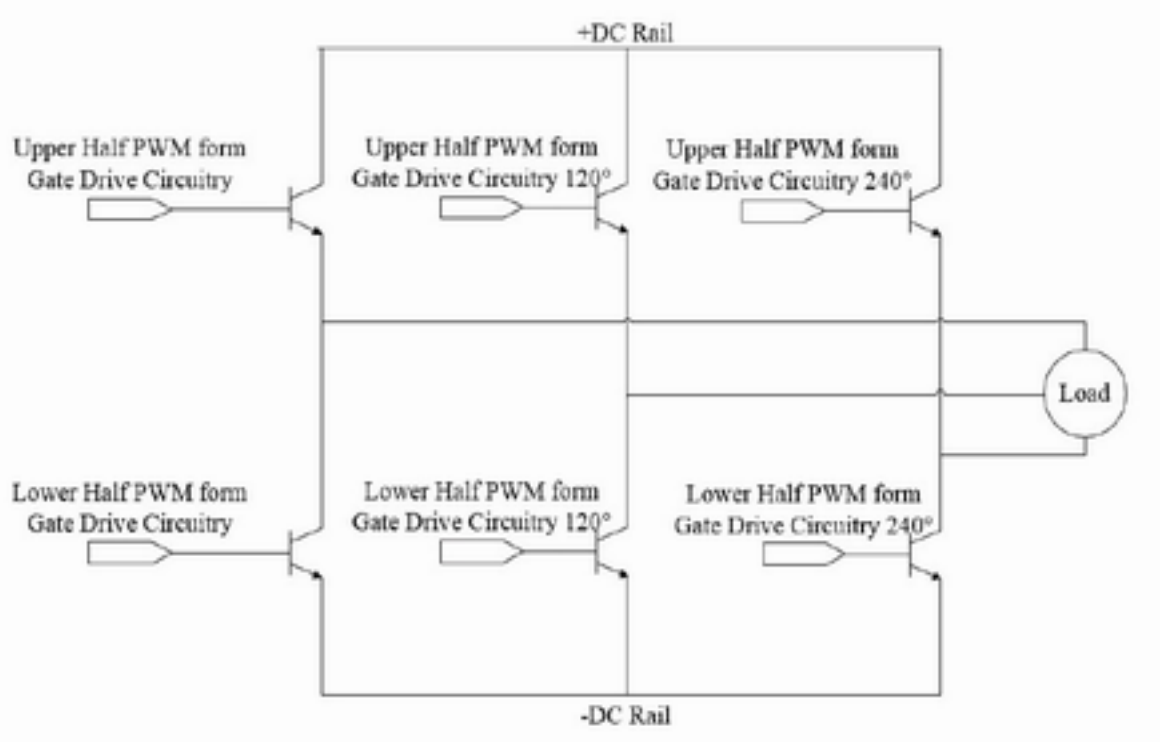

Figure 8: Three-Phase Inverter Configuration

The initial single-phase component shall:

- Be a Fairchild FMG2G75US60 IGBT (or equivalent) pair
- Each IGBT will receive one PWM signal (upper or lower, see figure 7 for clarification)
- Output one dual-sided PWM signal representing the necessary sine wave to the filter
- Have DC rails capable of providing 15 A of current

The subsequent (time permitting) three-phase component shall:

- Be comprised of three separate single-phase components, as shown in figure 8
- The three single-phase inputs shall be 120° out of phase from any other phase input
- Be capable of providing 5 A of current per phase

Filter:

The output of the inverter shall be passed through a filter before being sent to the load. The filter shall be used for the extraction of a sinusoidal wave represented in the dual sided PWM output from the Inverter. There shall only be one implementation iteration for the filter. This is because the filter that, time permitting, shall be used in the three-phase VFACS will be strictly composed of three single phase filters.

To perform this task, an LC filter design has been selected. It should be noted that figure 9 shows an ideal LC filter. A realizable filter of this configuration will also have a resistance associated with the inductor. The inclusion of this resistance would change the filter design from an ideal LC filter to a practical RLC filter. For information regarding the implementation of an RLC filter, refer to Appendix A. The filter is to be designed such that attenuation is minimal at 60 Hz

and maximized at 15 kHz, the switching frequency of the PWM signal. It should be noted that all frequency components of the PWM signal will be greater than or equal to 15 kHz.

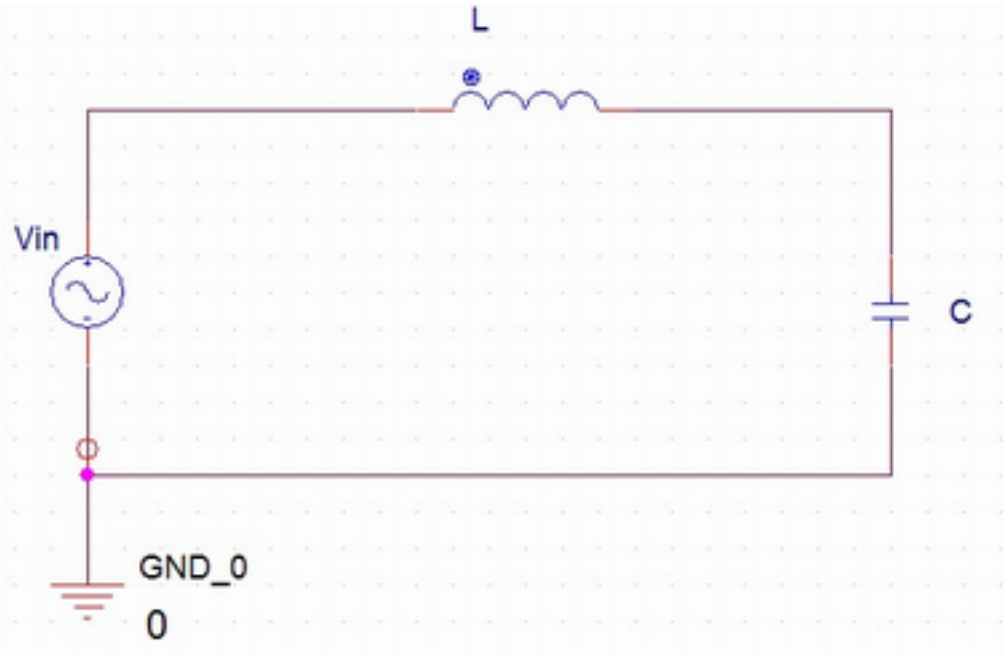

Figure 9: Ideal LC Filter Design

Equipment and Parts:

- LabVIEW Student Edition (still to be purchased)
- NI-cDAQ-9174 Data Acquisition Chassis
- NI-9401 Digital I/O Module
- NI-9221 Analog-to-Digital Converter Module
- NI-9211 Thermalcouple Module
- IR 2110 Gate Driver (limited numbers available in power lab)
- 6N137 Optical Isolator
- FMG2G75US60 IGBT Pair with anti-parallel diodes (three available)
- Sources and Scopes available in Power Lab

Schedule:

Table 2 represents a schedule of tasks for the spring 2014 semester. This schedule should put this project on track for completion with time included for documentation and presentations. The work division will be determined on a weekly basis and will be based on area of experience and efficiency of labor. Weeks 2, 4, and 5 will be critical work weeks because of the volume of work to be completed. The work during these weeks will be divided into parallel work paths to maximize the lab time available for the project.

Schedule		
Week	Date	Task
1	1/27/2013	LabVIEW Tutorials
2	2/3/2013	Build & test single phase optical isolator Build & test single phase gate driver and inverter
3	2/10/2013	
4	2/17/2013	Interfacing LabVIEW with NI cDAQ
5	2/24/2013	Basic LabVIEW controller design
6	3/3/2013	LC filter design & single phase resistive/inductive load selection
7	3/10/2013	Apply LC filter and load to single phase VFACS
8	3/17/2013	Controller tuning/modification with voltage feedback
9	3/24/2013	Performance testing of single phase VFACS
10	3/31/2013	Re-evaluation of schedule/evaluation of implementing three-phase VFACS
11	4/7/2013	DC to AC source conversion design
12	4/14/2013	DC to AC source conversion building and testing
13	4/21/2013	Final system testing and analysis
14	4/28/2013	Oral Presentation Preparation/ Final Project Report

Table 2: Spring Task Schedule

References

[1] A. Thomas, "dSPACE DS1103 Control Workstation Tutorial and DC Motor Speed Control" November 2008.

[2] C. Edwards, E. Smith, "Design of Simulink-Based 2-DOF Robot Arm Control Workstation" October 2006.

[3] (June 2000) AC Drives Using PWM Techniques. [Online] Available: http://literature.rockwellautomation.com/idc/groups/literature/documents/wp/drives-wp002_-en-p.pdf

[4] K. Gavelek, V. Panek, C. Smith, "Closed Loop Control of Halbach Array Magnetic Levitation System Height (CLCML)" October 2012.

[5] http://en.wikipedia.org/wiki/RLC_circuit

Appendix A: RLC Filter Design

Transfer Function:

$$\frac{V_o}{V_i} = \frac{\frac{1}{LC}}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$$

Break Frequency:

$$w_0 = \frac{1}{\sqrt{LC}}$$

Fractional Bandwidth:

$$F_b = \frac{\Delta\omega}{\omega_0} = \frac{1}{Q}$$

Bandwidth:

$$\Delta\omega = 2\alpha$$

Damping Factor:

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}}$$

General RLC Filter Layout and Frequncy Resonce.