Variable Frequency AC Source

Functional Requirements List and Performance Specifications

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Introduction:
Variable frequency drives (VFDs) are commonly used in systems with AC motors requiring speed control (e.g., conveyor belts, pumps, pulleys). VFDs are generally comprised of the following four subsystems:

- AC to DC Rectifier
- DC Signal Conditioner (low pass filter)
- Inverter
- PWM Generator

The four subsystems work in combination to modify the frequency of the standard US 60[Hz] power signal for use in various system applications involving AC induction motors. VFDs also maintain the constant volts/hertz ratio needed to limit motor current and provide the required torque on the load as the speed is varied. Without a constant volts/hertz ratio, the motor current would increase at lower frequencies (i.e., less than 60[Hz]), potentially decreasing motor reliability.

Project:
The goal of this project is to design and construct a Variable Frequency AC Source (VFACS) that can be used as a platform for the development of a Variable Frequency Drive. The system will initially be developed for a single phase source, but will be extended to a three phase source if time permits. Our subsystem goals for this project are as follows:

- Development of the PWM Generation Controller with LabVIEW
- Design and Implementation of Gate Drive Circuitry
- Design and Implementation of the Inverter with Gate Drive Circuitry
- Closed-loop control for voltage

The overall goal for the project is to produce a Variable Frequency AC Source with these subsystems that will be able to drive a single phase load. Again, if time permits, a three phase VFACS will be attempted.

High Level Block Diagram:
The high level system block diagram for the VFACS is shown in figure 1. The system will be comprised of the following five subsystems:

- PWM Generation Controller
- Gate Drive Circuitry
- Inverter
- Filter
- Load

The only input to the VFACS system will be the desired inverter output frequency delivered to the load, and the only output will be the motor speed. The subsystems will have interconnections as detailed in table 2.

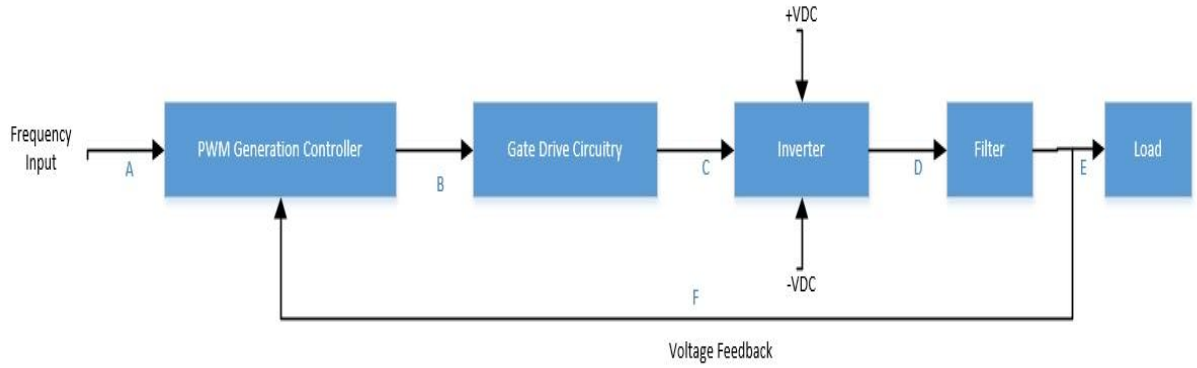

Figure 1: VFACS High Level System Block Diagram

VFACS Subsystem Connection Lists					
	Subsystem	**# of Inputs**	**Inputs**	**# of Outputs**	**Outputs**
1	PWM Generation Controller	2	Frequency Input Load Voltage Feedback[1]	4	Gate Drive Circuitry
2	Gate Drive Circuitry	4	PWM Gen. Controller	4	Inverter
3	Inverter	4	Gate Drive Circuitry	1	Filter
4	Filter	1	Inverter	1	Load
5	Load	1	Filter	1	PWM Gen. Controller*

*Feedback to the PWM Generation Controller will be measured at load terminals using a Nat. Instru. cDAQ

Table 1: VFACS Subsystem Connection (I/O) List

Pulse Width Modulated (PWM) Generator:

This component shall create a PWM signal which shall:

- Be generated based on a frequency input from the user and a voltage feedback from the load
- Output to the gate drive circuitry
- Be produced using a LabVIEW based cDAQ controller from National Instruments
- Represent a sine wave ranging from 0 to 400 Hz
- Be produced by comparing a sine wave and two triangle waves as seen in figures 2 & 3
- Use two 15 KHz triangle waves and a variable amplitude and frequency sine wave from 0 to 400 Hz
- Produce a constant V/Hz ratio of 0.5892 at and below 60 Hz, reference figure 4 for a normalized plot of this ratio

[1] These components may change based on performance during testing

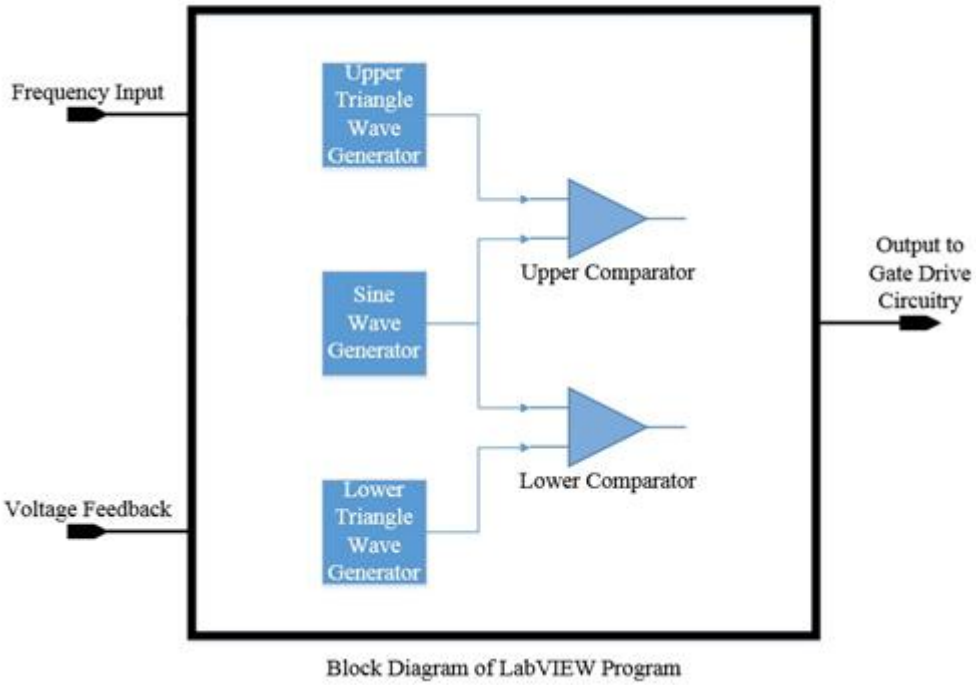

Figure 2: LabVIEW PWM Generator Block Diagram

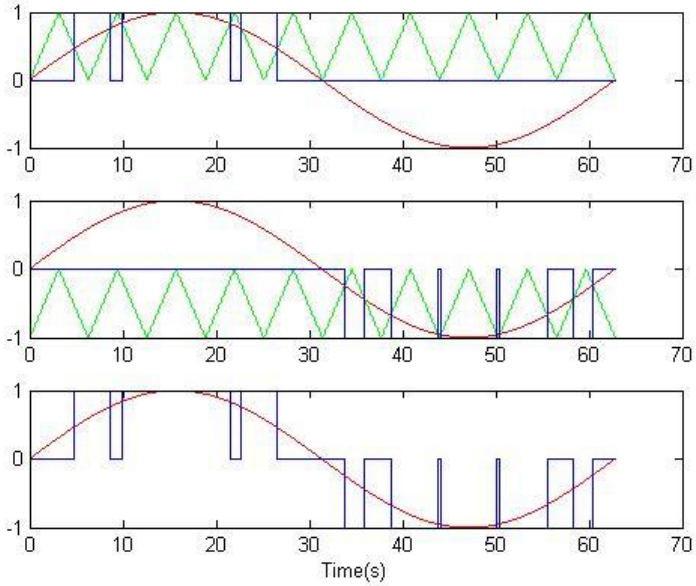

Figure 3: Examples of Sine, Triangle, and PWM Waveforms

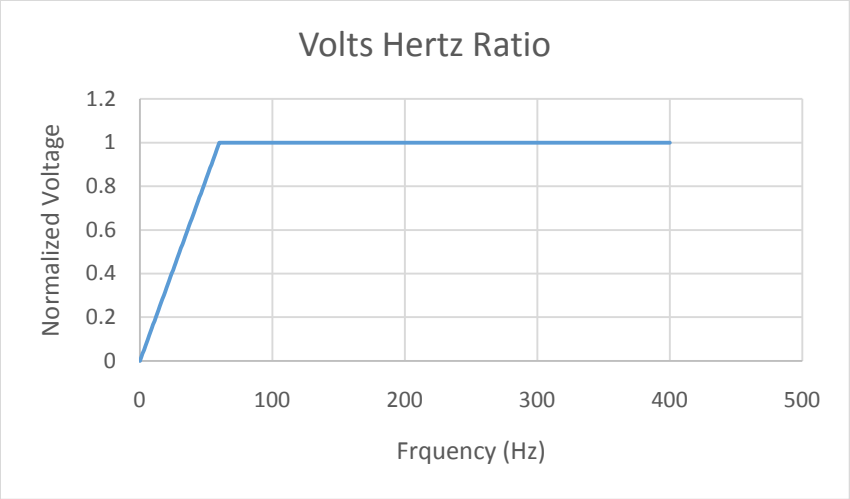

Figure 4: Normalized Volts/Hertz Ratio

Gate Drive Circuitry:
This component shall:

- Use a *6N137 optical isolator
- Use a *IR 2110 gate driver to drive the IGBTs in the inverter
- Receive TTL level inputs from the PWM generator
- Provide 0 to 15 V outputs to the transistors
- Minimize clipping at 1% duty cycle of the 15 KHz PWM signal
- Have one gate drive circuit per IGBT pair of the inverter

Inverter:
The initial single-phase component shall:

- Be a Fairchild FMG2G75US60 IGBT (or equivalent) pair
- Each IGBT will receive one PWM signal (upper or lower, see figure 5 for clarification)
- Output one dual-sided PWM signal representing the necessary sine wave to the filter
- Have $\pm$ 50 VDC relative rails capable of providing 15 A of current

The subsequent three-phase component shall:

- Be comprised of three separate single-phase components, as in figure 6
- The single-phase inputs shall be 120° out of phase from any other input
- Be capable of providing 5 A of current per phase

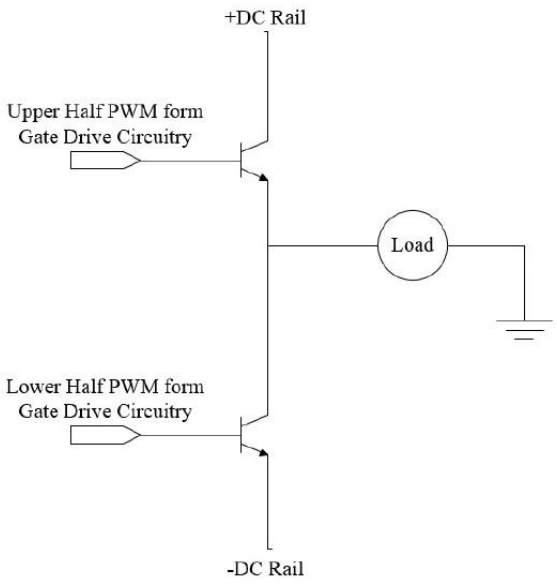

Figure 5: Single Phase Inverter

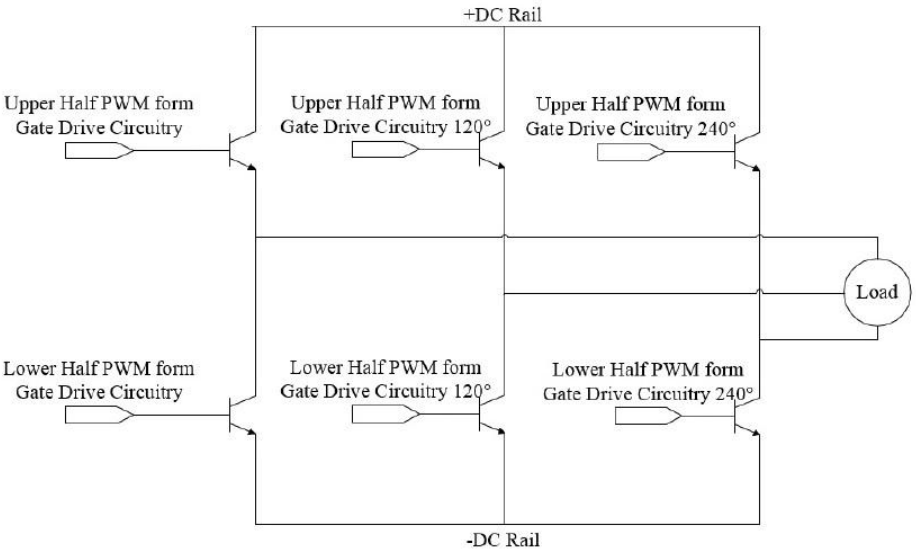

Figure 6: Three Phase Inverter

Filter:

This component shall:

- Be a lowpass LC filter
- Allow less than 0.5 dB attenuation between 0 and 400 Hz
- Utilize components rated for 100 VRMS and 15 ARMS
- Output a sinusoidal waveform extracted from the PWM signal

Load:
The single-phase load shall:

- Receive a single, filtered sinusoidal input
- Be resistive in nature
- Be used only for testing and system verification
- Be rated for 100 VRMS and 15 ARMS

The three-phase load (if time permits) shall:

- Receive a three-phase sinusoidal input
- Provide voltage feedback for the PWM generator
- Initially be resistive for testing
- Subsequently drive an inductive motor
- Be rated for 100 V and 5 A