Ultrasonic Signal Processing platform for Non-destructive Evaluation

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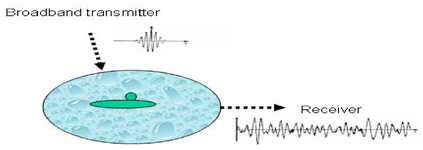
Motivation

- Ultrasonic non-destructive evaluation (NDE) has been widely used in quality assessment and failure analysis for critical structures or components in manufacturing, bridge structure, microelectronic packaging, and composite materials for aircraft structure.



- Ultrasonic Platform:
  - Requires hardware adaptability
  - Demands high speed performance
  - Handles versatile signal processing

Objectives

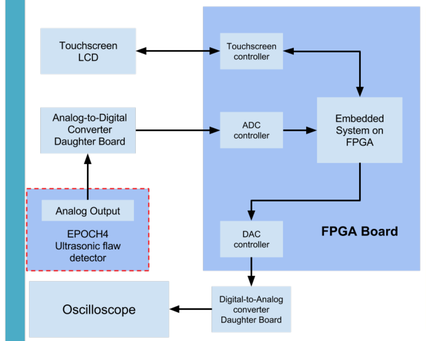
- Design an Ultrasonic Signal Processing Platform
- Preform data acquisition
- Implement on a Field Programmable Gate Array(FPGA)
- Modularity for future design extension

Project Goals

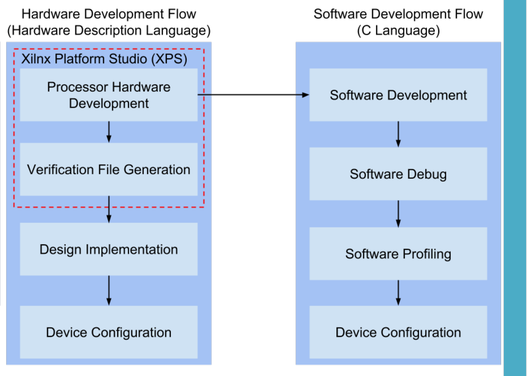
- Preform system Integration of:
  - Virtex-5 LX110T FPGA development board
  - 12-bit Analog to Digital Converter (Up to 170 MSPS)
  - 14-bit Digital to Analog Converter (Up to 200 MSPS)
  - Amulet STK480272C Touchscreen (Resolution: 408x272, Serial Communications)
- Implement system using Xilinx embedded development tools
- Evaluate split spectrum processing algorithm(SSP)

Ultrasonic Signal Processing Platform

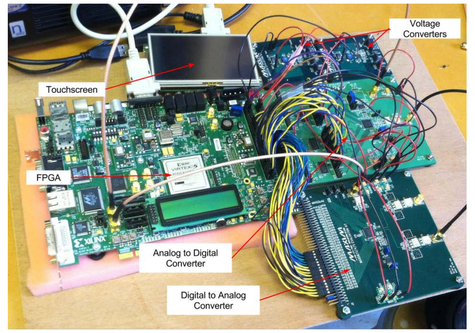
System Block Diagram



Embedded System Design Flow for FPGA Implementation [1]



System Setup



- The Virtex-5 FPGA hosts the embedded system and interfaces to all peripherals
- The ADC board provides 12-bit differential signals for data acquisition. The FPGA board performs single-ended conversion.
- The DAC board accepts 14 single ended signals from the FPGA.
- Coaxial SMA cables used for clock connections.
- Voltage converters: 3.3v → 1.8v
- RS232 communication for the touchscreen.

Preliminary Results

Digital to Analog Converter

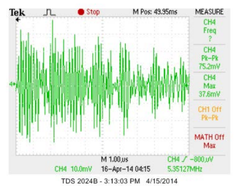


Figure 1. Experimental Ultrasonic Data

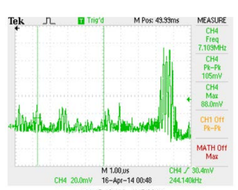


Figure 2. Signal Processing Result

Analog to Digital Converter

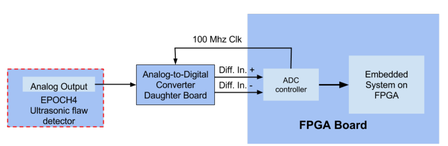


Figure 3. ADC Interface Diagram

Touchscreen

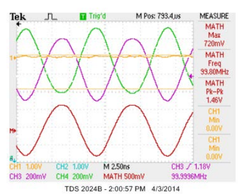


Figure 4. Differential Clock Outputs

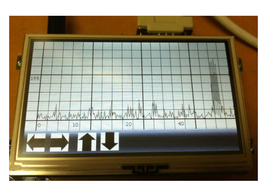


Figure 5. Signal Processing Result

ADC and DAC Data Loopback

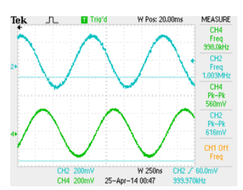
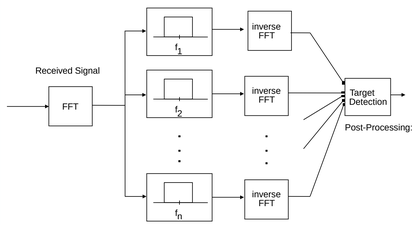
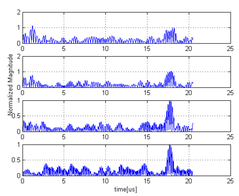


Figure 6. Loopback signals

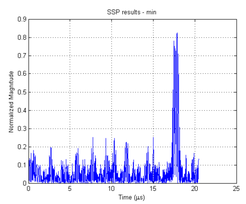
Split Spectrum Processing Algorithm



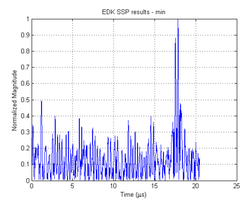
SSP Block Diagram [2]



Multi-channel Signals(Matlab)



Signal Processing Results(Matlab)



Signal Processing Results (FPGA)

Conclusion

A reconfigurable Ultrasonic Signal Processing Platform has been implemented using C and VHDL. It can run at 100 MSPS for data acquisition. Split spectrum processing algorithm has been successfully evaluated on the system. The results from the FPGA and MATLAB have been compared. The platform, including all design modules, can be used for future projects in communication and signal processing.

References

[1] Xilinx (2011, April 13). *EDK Concepts, Tools, and Techniques*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/edk_ctt.pdf

[2] J. Saniie, E. Orkulu, and S. Yoon, "*System-on-Chip Design for Ultrasonic Target Detection Using Split-Spectrum Processing and Neural Networks*," IEEE Transactions on UFFC, vol. 58, no.7, pp. 1354-1368, July, 2011

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