Ultrasonic Signal Processing Platform for Nondestructive Evaluation

(USPPNDE)

Senior Project Final Report

Raymond Smith

Advisors: Drs. Yufeng Lu and In Soo Ahn

Department of Electrical and Computer Engineering
Bradley University, Peoria IL

May 12, 2014

ABSTRACT

Ultrasonic nondestructive evaluation (NDE) has been widely used in quality assessment and failure analysis in industrial applications. To meet the demands of high speed and requirements of adaptability in ultrasonic NDE signal processing, a reconfigurable computing device is highly desirable for the system implementation. Without requiring hardware changes, the use of a Field Programmable Gate Array (FPGA) expands the product life by updating data stream files. Additionally FPGAs have grown to have the capability to hold an entire system on a single chip.

In this project, an FPGA-based platform for ultrasound signal processing application has been developed. The platform is not only capable of performing high speed data acquisition at 100 MSPS, but also flexible enough to evaluate new signal processing algorithms and new NDE standards/methods. Split spectrum processing algorithm is implemented to evaluate the platform. Signal processing results can be displayed on an oscilloscope through digital-to-analog converter. They also can be redirected to a touch screen LCD for a demonstration purpose. This project may have a broader impact on capstone designs in signal processing applications.

Key words: *Ultrasonic NDE, FPGA , signal processing, data acquisition*

TABLE OF CONTENT

		Page
I.	Motivation and project goals	4
II.	System description	6
III.	Results and analysis	17
IV.	Conclusion	20
V.	Acknowledgement	20
VI.	Reference	21

I. Motivation and project goals

Ultrasonic nondestructive evaluation (NDE) has been widely used in quality assessment and failure analysis for critical structures or components in manufacturing, bridge structure, microelectronic packaging, and composite materials for aircraft structure. In the ultrasonic NDE, the detected echoes are often random, interfere with each other and also may be contaminated by noise. Hence, it becomes challenging to use the backscattered echoes in order to unravel the desired information necessary, such as location, boundaries, orientation, and size of defects, for material characterization and structural health monitoring. Various signal processing algorithms have been developed to characterize non-stationary and nonlinear behavior of ultrasonic signals for NDE Applications. Extensive research in ultrasonic signal processing such as chirplet signal decomposition, Hilbert-huang transform, empirical mode decomposition (EMD), active noise cancellation, and Fractional Fourier transform have been conducted in the Department of Electrical and Computer Engineering at Bradley University[1-5]. Besides developing better signal processing algorithms, there is another important aspect of the challenges in ultrasonic industrial applications. That is, how to implement these algorithms efficiently on hardware. The nature of NDE requires a lot of fieldwork for NDE operators. A flexible real-time ultrasonic signal processing system has a significant impact in all these applications.

A conventional hardware design based on microcontrollers and digital signal processor falls short of meeting the demands of high speed, and adaptability requirements. This necessitates reconfigurable computing devices such as Field Programmable Gate Arrays (FPGA) to implement hardware and software co-design for the ultrasonic system.

FPGA is widely used in embedded applications such as automotive, communications, industrial automation, motor control, medical imaging etc. Without requiring hardware change-out, the use of FPGA type devices expands the product life by updating data stream files. It has grown to have the capability to hold an entire system on a single chip; meanwhile, it allows in-platform testing and debugging of the system. Furthermore, it offers the opportunity of utilizing hardware/software co-design to develop a high performance system for different applications by incorporating processors

The goal of this project is to build a prototype ultrasonic NDE system, which has features listed as follows.

1. It acquires ultrasonic data at 100 MSPS.
2. It should be flexible so that future needs such as new signal processing algorithms and new nondestructive evaluation standards/methods, and new features can be added without re-designing the whole system in hardware.
3. A touch-screen LCD will be used as a display module of the whole system.

In addition, the designed system may be used as a general research and educational platform for communication and signal processing projects at Bradley University.

The whole project report includes the following sections. Section II describes the system using block diagrams. Section III discusses subsystems including data acquisition subsystem, LCD touchscreen subsystem and signal processing subsystem, where split spectrum processing algorithm is used as an example for the purpose of demonstration. Section IV analyzes and discusses the project results. Section V concludes the report. VI lists all references.

II. System description

Figure 1 shows a block diagram of a typical ultrasonic NDE data acquisition system.

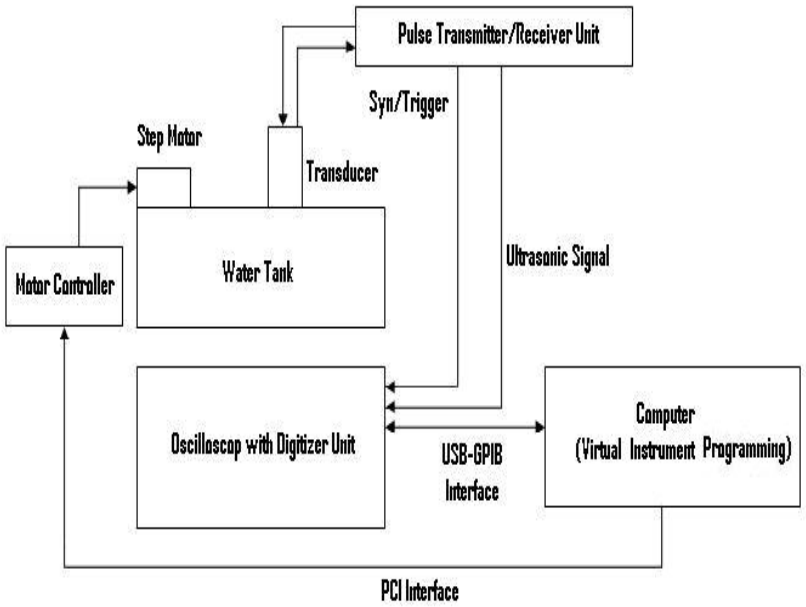

Figure 1. Typical block diagram of an ultrasonic NDE system [3]

It can be divided in to two subsystems. One is data acquisition subsystem, including Oscilloscope with digitizer unit, pulse transmitter/receiver unit, transducer, and virtual instrument program running on a computer. Another is positioning subsystem, including motor controller and step motor. A similar system is commonly used to collect experimental data in research labs. MATLAB or C program is written to post process the collected data for advance signal processing algorithms. It is challenging to combine these two steps (i.e., data acquisition and signal processing) together. Usually an algorithm-specified system is carefully designed.

In this project, the FPGA-based system is shown in Figure 2.

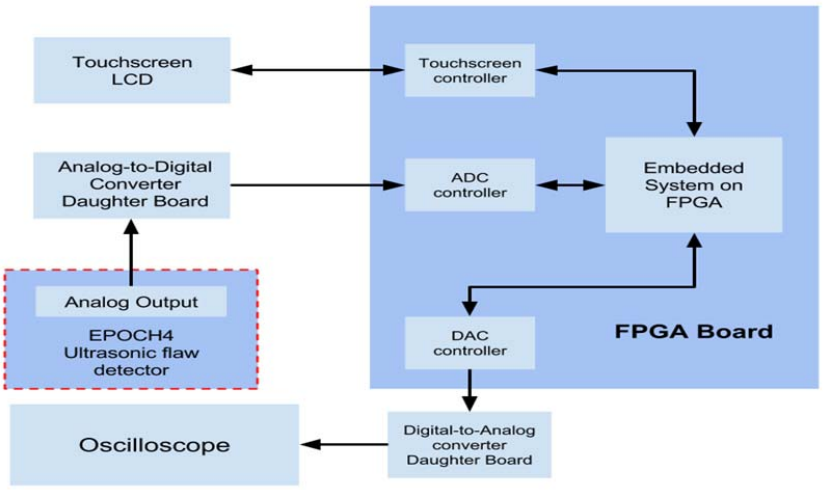

Figure 2. Block diagram of proposed ultrasonic signal processing platform

It can be seen that the system mainly includes an FPGA board, a touchscreen board, an analog-to-digital board and a digital-to-analog board. In this project, XUP Virtex 5 FPGA development board and Genesys FPGA board are utilized to debug and implement the system. Both boards are donated by Xilinx, the industrial leading company of FPGA. In addition, through Xilinx University Program, Xilinx provides professional level software packages for simulation, synthesis, design and implementation. High-speed data acquisition boards (MAX5874 and MAX1213N) from Maximum Integrated Inc. are used to perform analog-to-digital conversion and digital-to-analog conversion. They run at 100M samplers per second in the implemented system. An Amulet STK touchscreen LCD is used to display results. An embedded system is designed to run on the Viretex 5 FPGA. It uses a 32-bit Microblaze processor running at 100 MHz, saves incoming data from ADC to the external DDR memory, and accepts the inputs from the GUI running on the touchscreen. C language is used to design the drivers of peripherals and VHDL is used for the design of lower-level controlling components. The overall system is illustrated in Figure 3 below.

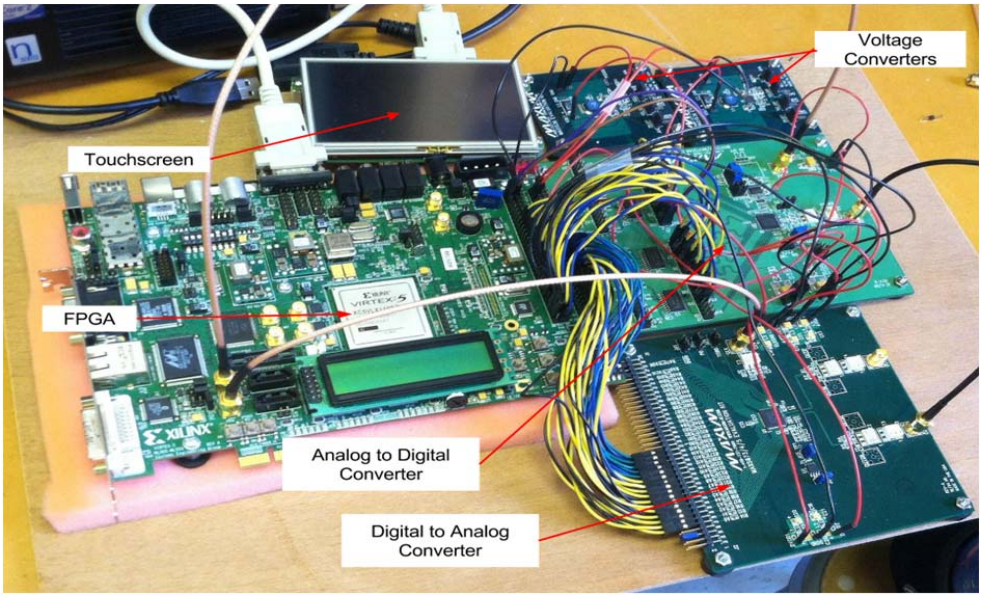

Figure 3. Ultrasonic NDE signal processing platform

The design flows using VHDL and C languages for hardware implementation and software realization of the system are shown in Figure 4. The design package is Xilinx 14.5 ISE suite including Project navigator, embedded development kits (EDK) and software development kits (SDK). Additionally, Chipscope, an on-chip debugging tool, is used for design troubleshooting.

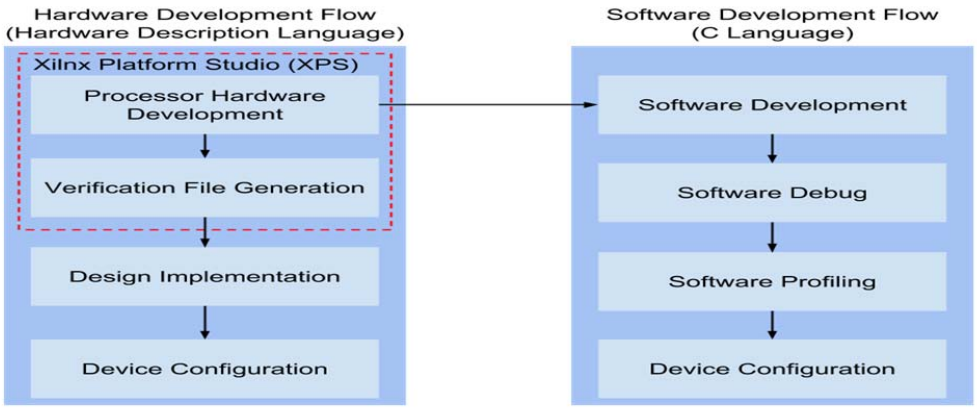

Figure 4. Design flow using VHDL and C language

Data acquisition subsystem

Specifications of FPGA board, digital-to-analog converter(DAC)board, and analog-to-digital(ADC) board are listed below[6-8]:

FPGA Board (Genesys Virtex-5 XC5VLX50T)

- The main board in the system to be developed
- Interface with DAC and ADC peripherals
- Interface with the touchscreen LCD board through UART
- Running under 100 MHz on-board system clock
- Others: 256 MB DDR2 memory, 32 MB flash memory and multiple USB2 ports.

DAC board (MAX5874 EVKIT)

- MAX5874: A 14-bit, high-dynamic-performance DAC from Maxim Integrated, Inc.
- Support update rates of 200 M samples per second.
- Operate under 3.3V and 1.8V supplies provided by the FPGA board and a MAX1536 voltage converter.
- Controlled by the 100 MHz clock signal from the FPGA board.
- Output a single-ended analog signal between 0 and 2Vpp

ADC board (MAX1213N EVKIT)

- MAX1213N: 12-bit low power ADC from Maxim Integrated, Inc.
- Support a sampling rate up to 170 M samples per second.
- Operate under 3.3V and 1.8V supplies provided by the FPGA board and a MAX1536 voltage converter.
- Controlled by the 100 MHz clock signal from the FPGA board.
- Accept a single ended analog input signal between 0 and 2Vpp (EPOCH 4 ultrasonic flaw detector provides the analog signal source)
- Output 12 differential LVDS2.5 signals

During the project, there are some issues or key points to get connection and wiring right for all these daughter boards and FPGA board. It takes a great amount of time to identify and solve them. There are lessons learned in the project. Some of them are described below.

1. The analog ground and digital ground should be separated so that the noise can be better controlled.
2. The clock from FPGA to DAC and ADC daughter boards runs at 100 MHz. The interference of high frequency noise deteriorates the signal. To solve the problem, RF SMA Cables were used for direct connection of clocks. It greatly reduces the noise level.
3. The output signals from ADC are in the format of LVDS (low-variance differential signal). For instance, 12 pairs of data bus (i.e., 24 signals) are used to represent 12-bit data. To use the 12-bit data in the signal processing algorithm running on the embedded system, VHDL codes are written to convert differential signal to single-ended signal. It is the first time to handle differential signal in the practical design using VHDL. There is similar data conversion in the DAC part.

As a demonstration, differential clocks and single-end clock are outputted to an oscilloscope

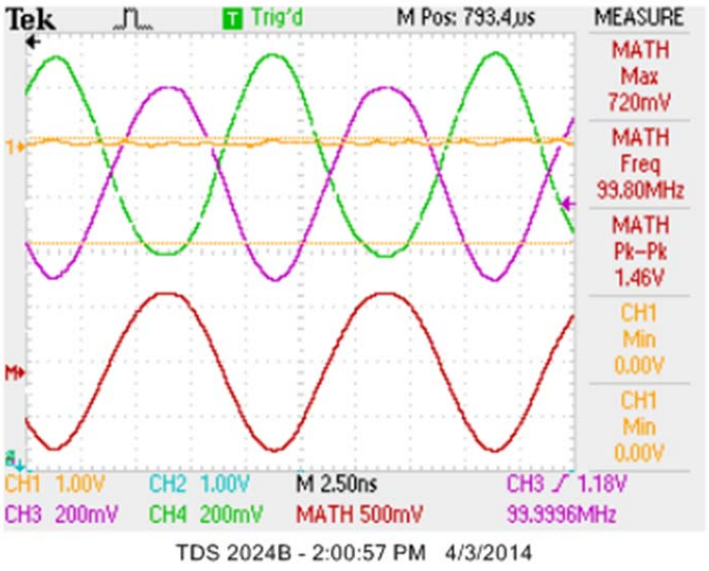

Figure 5. oscilloscope output showing the ADCs two LVDS clock outputs.
This output verifies that the ADC is receiving the clock output from the FPGA over SMA properly.

To conclude the description of data acquisition system, a few testing have been completed and the results are shown in the following figures.

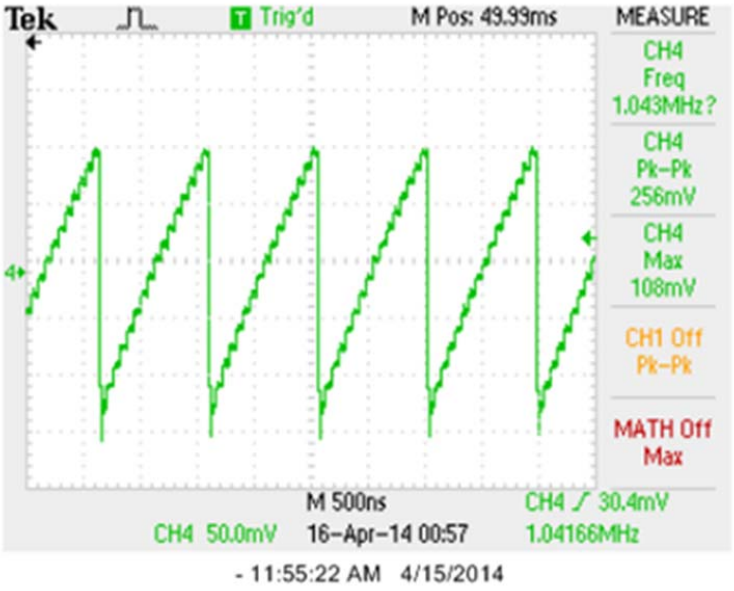

Figure 6. A sawtooth waveform generated in VHDL that was used to test the DAC

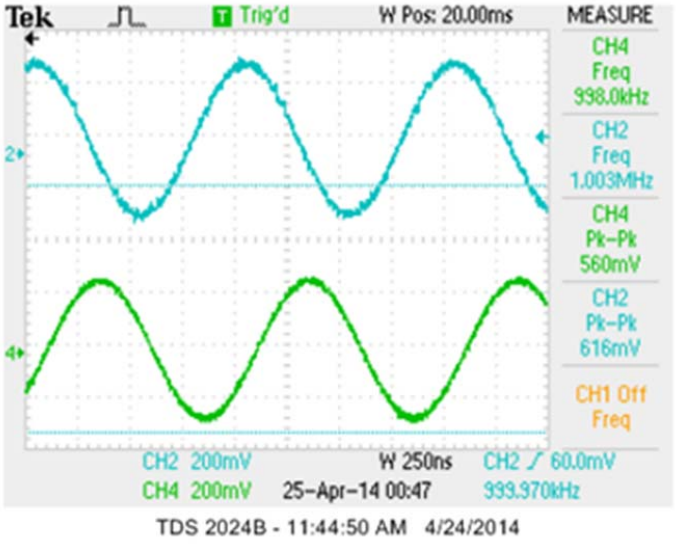

Figure 7. loop back of a sinusoid between ADC and DAC devices.
The green signal is the input into the ADC. The blue signal is the output of the DAC.

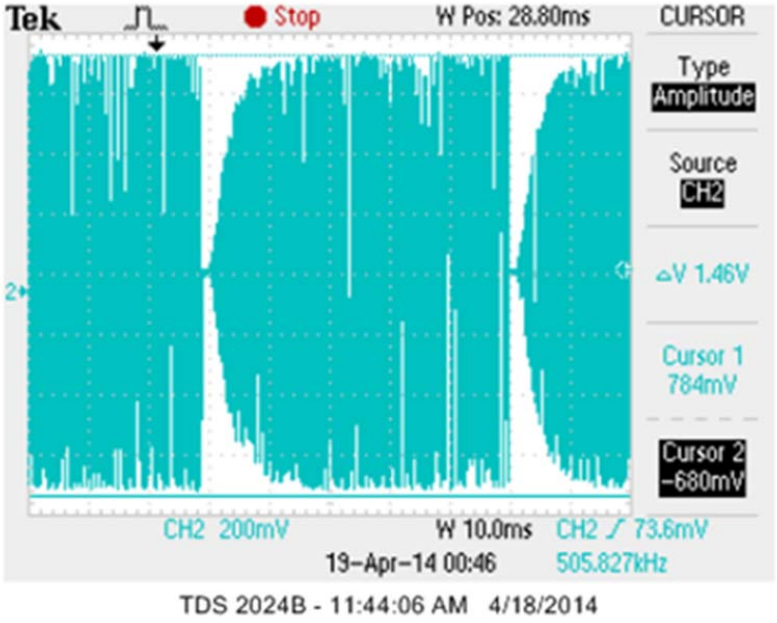

Figure 8. Loop back of a Chirp from 10 kHz to 10 MHz

Touch-screen subsystem

The specification of the touch screen is listed below[9].

LCD touch screen (Amulet STK-480272C)

- A LCD touch screen board used in past senior projects.
- Serial port communication protocol with 115200 BAUD rate
- Used as a peripheral of the embedded system running on the FPGA board.
- Other specifications: 480 X 272 resolution, refresh rate at 100 Hz.

The flow chart of communication protocol is shown in Figure 10.

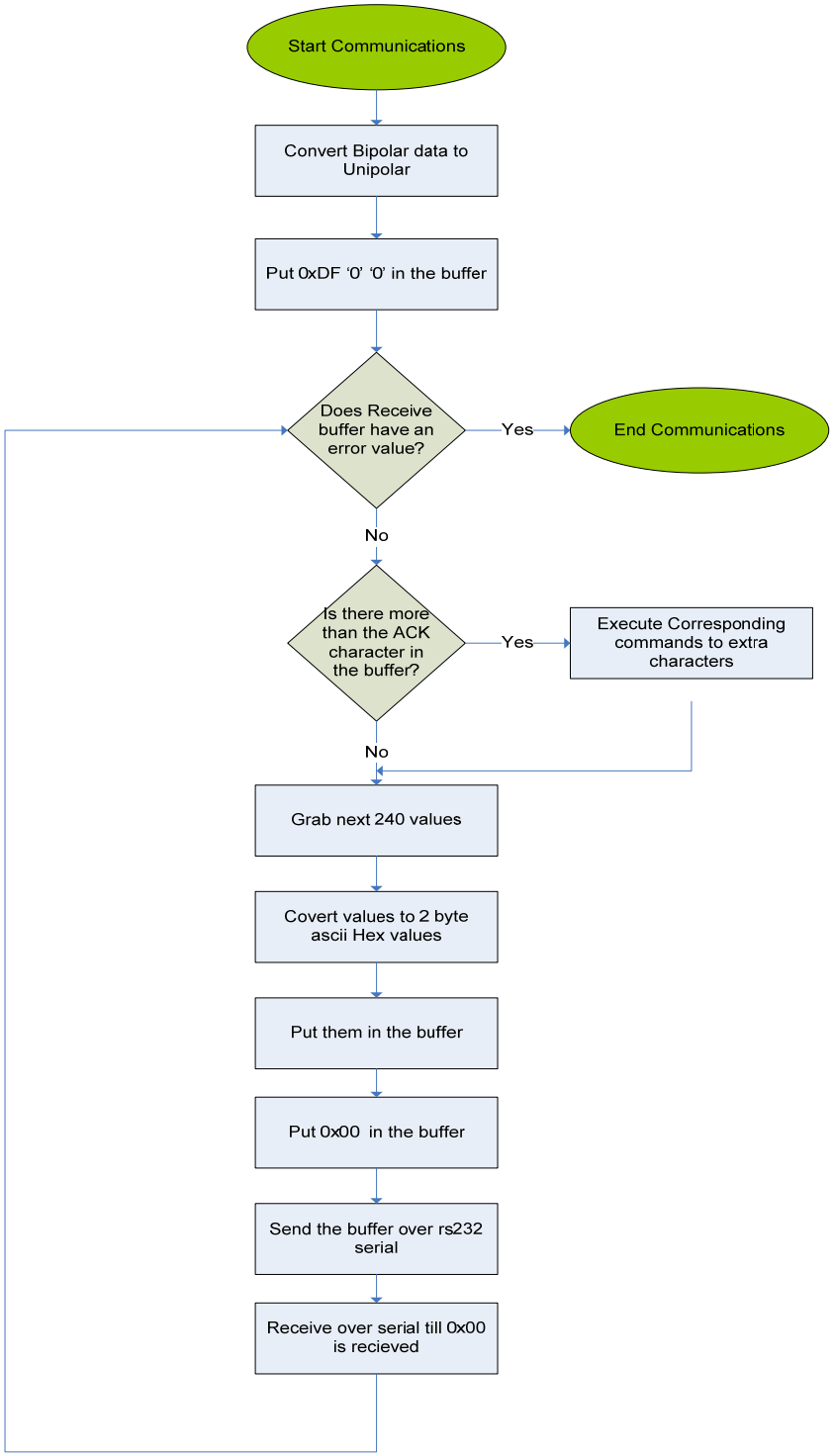

Figure 10. Communication protocol of LCD touchscreen

Signal processing on FPGA

The split spectrum processing (SSP) algorithm [11] has been implemented in C. The algorithm was tested in MATLAB then implemented in SDK in C. The algorithm works properly, but takes upwards of 50 seconds to complete. Currently the system is simply too slow to interface with the system at the rate data is being sampled. It would be ideal to switch some aspects of the function, especially the FFT and nonlinear filtering to hardware processes in VHDL. The issue comes from floating point operations. Switching to fixed point logic would speed the process up, but it would be easier to use an existing FFT IP core and get an even larger boost of speed than moving the function to fixed point. Post processing of the filter banks could also be done in parallel in hardware to speed up the system. To operate as fast as data is being sampled the processing would need to be able to operate around 1 million times a second Further work will have to be done to identify how much the hardware implementation if the split spectrum processing algorithm will yield a sufficient speed increase to make the algorithm viable. If it is not viable the input data set will have to be reduced, by narrowing the time window analyzed around the echo. Nevertheless, the whole point of SSP algorithm implementation is to show the feasibility of the FPGA platform. For the improvement of performance, there are a lot of work can be done in the EDK design environment. It is worthy to point out that the realization for different algorithms does not need an overhaul of hardware. The EDK package allows the flexibility of design change through software.

The SSP algorithm and its MATLAB simulation results are shown in the figures below.

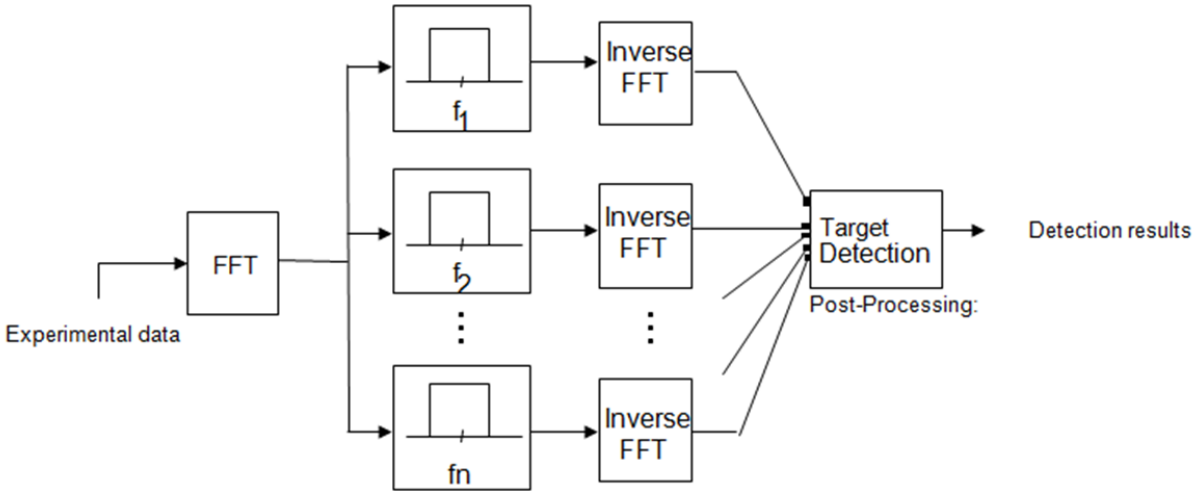

Figure 10 Split spectrum processing algorithm diagram

Figure 10 shows the diagram of SSP algorithm. The experimental data is converted in the frequency domain through FFT, and then multiple frequency bands have been applied to filter the signal. After IFFT operation on each frequency band, a nonlinear filtering is used for target detection. Figure 11 shows the raw ultrasonic data, where a 5MHz transducer is used. Furthermore, Figure 12 shows the signals in different frequency bands and the final processing results is shown in Figure 13.

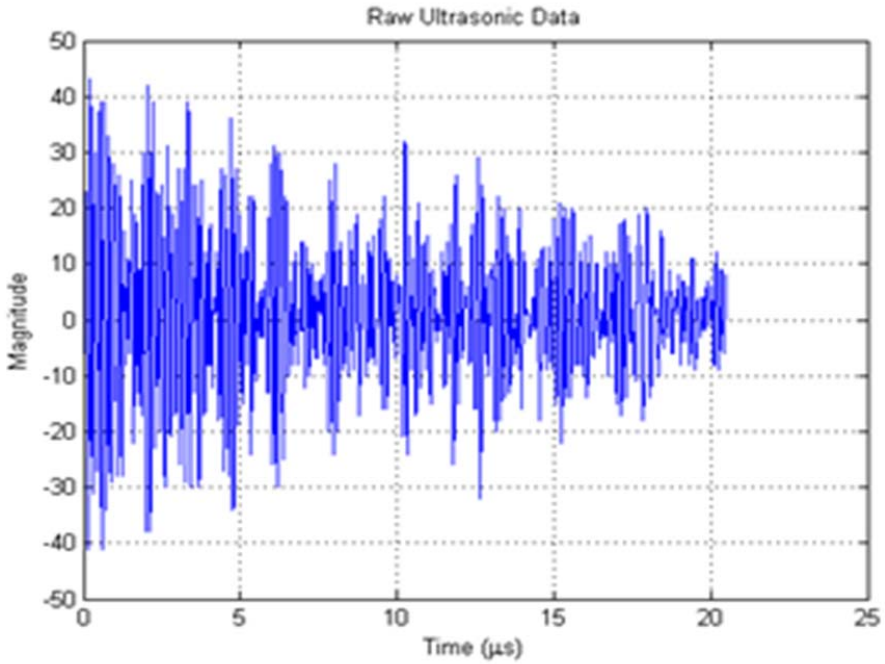

Figure 11 Raw ultrasonic data (5 MHz Transducer)

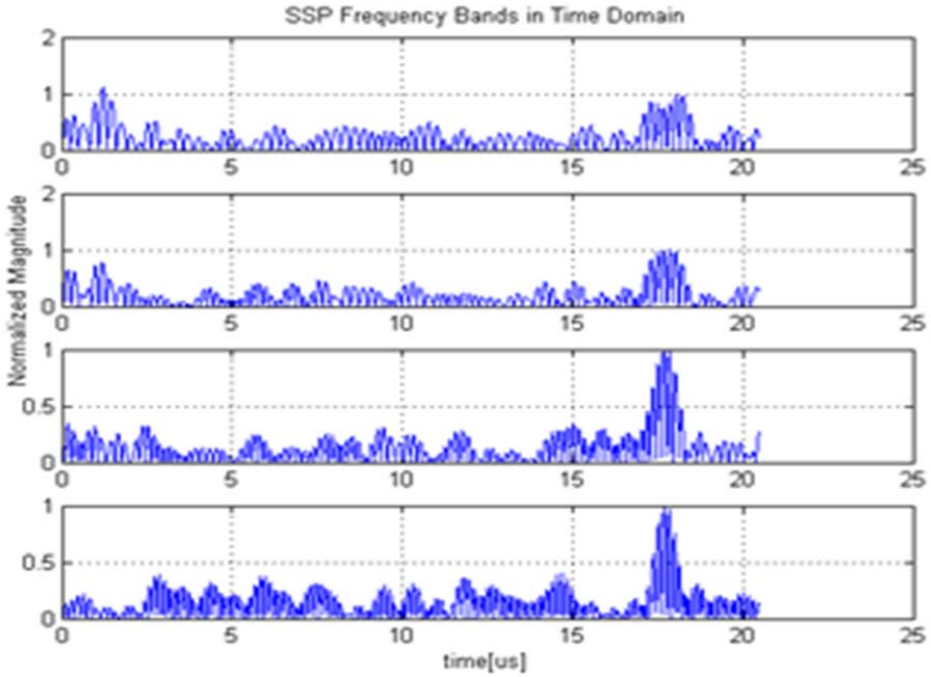

Figure 12. Signals in different frequency bands of SSP

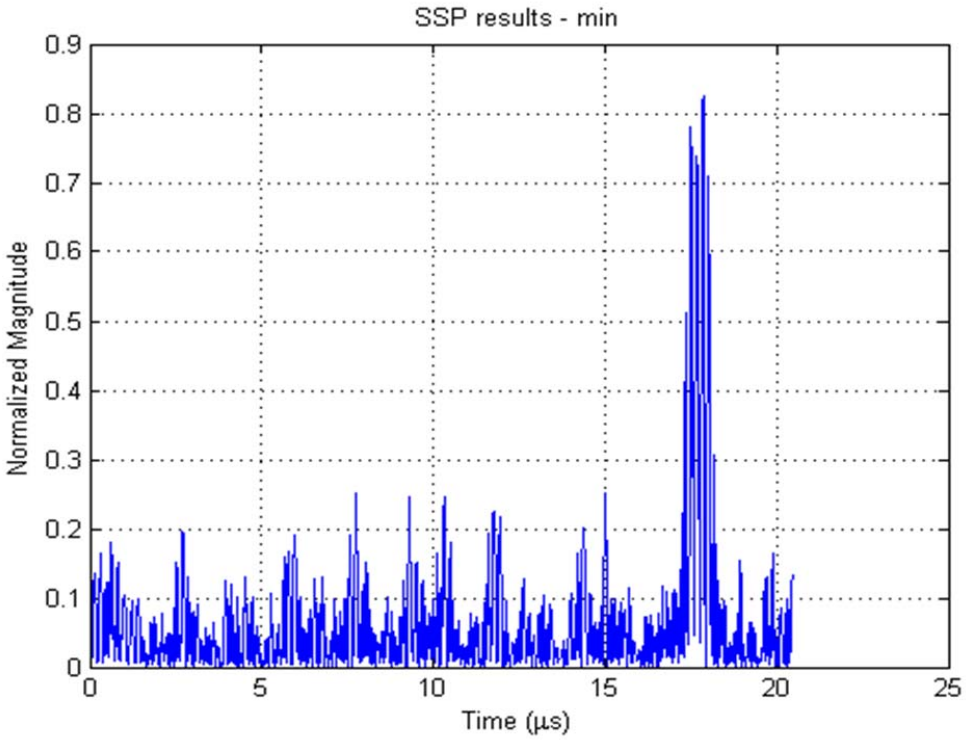

Figure 13. Signal processing result of raw data using SSP (Raw data is plotted in Figure 11)

III. Results and analysis

The whole embedded system runs on the FPGA. Each peripheral has had a controller implemented in C or VHDL. The hardware has been connected properly and operates in conjunction with each other. The split spectrum processing algorithm has been evaluated. Some of results have been shown in previous sections. The LCD touch screen interface has been completed in the summer of 2013. A VHDL implementation of the DAC controller has been completed and the results are as expected. To work properly the clock being supplied to the board had to be set to the LVCMOS_25 voltage standard and buffered through the one of the clock buffer instantiation templates such as BUFG, IBUFG, or BUFR in VHDL. 12 bit data from the ADC has been converted to 14 bits by placing the 12 data bits in the 12 most significant locations. Multiple signals have been sent to the DAC and observed on the oscilloscope as expected. Some of the results of the system are shown in Figures 2-4 below. Further work needs to be done to implement the VHDL as a peripheral to the embedded system. This includes code to access the correct locations in DDR2 memory as the ADC streams data into the system.

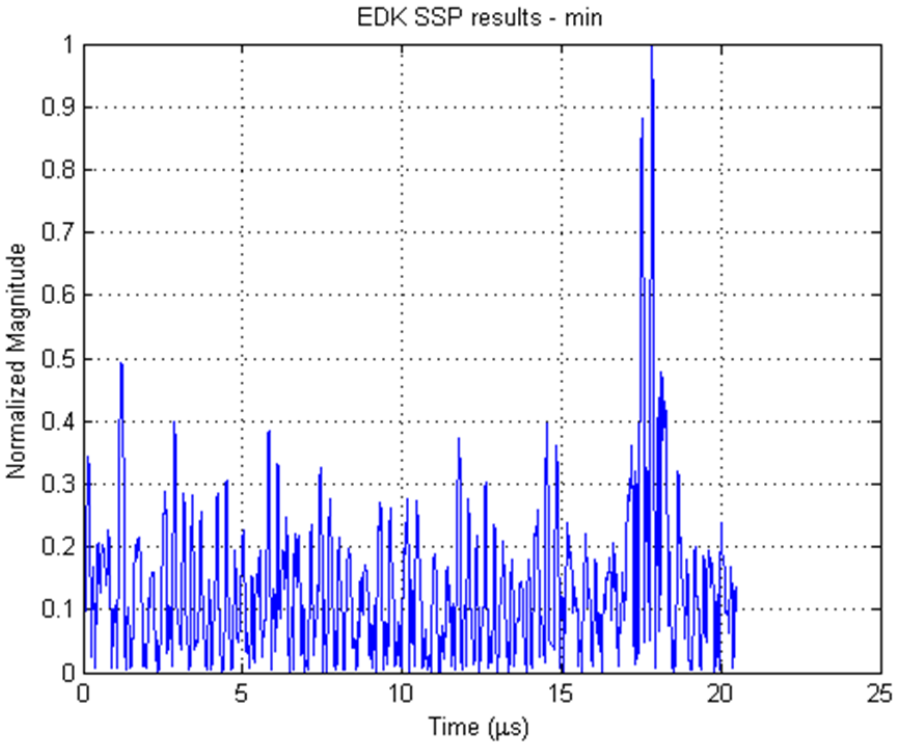

Figure 14 The SSP result from the C implementation in the EDK

Figure 14 shows the SSP result from the C implementation in the EDK. The result is captured and plotted in MATLAB. To demonstrate the overall system, the DAC is used to output analog signals so that they can be displayed on an oscilloscope. Figure 15 shows the output of experimental data and Figure 16 shows the result of SSP algorithm. It turns out that the results from EDK running on the FPGA boards match well with those from MATLAB. The LCD touchscreen is used to display the result as well. The result is shown in Figure 17.

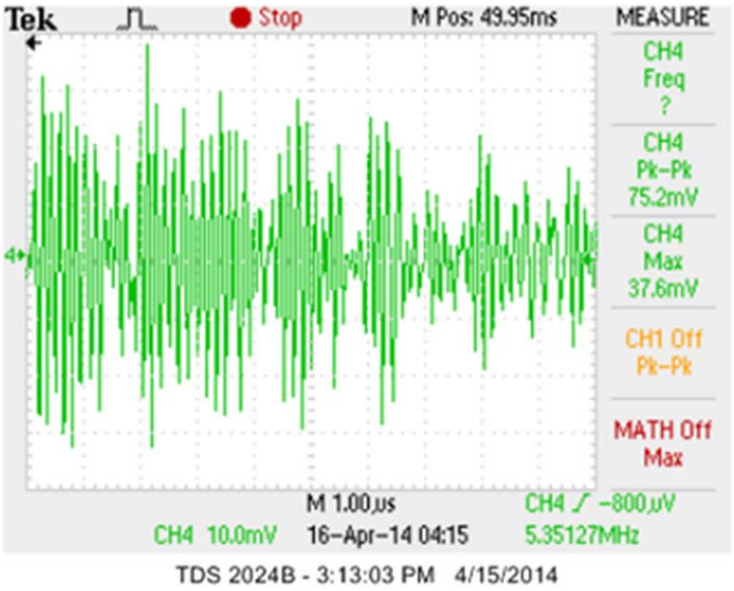

Figure 15. Oscilloscope output showing raw ultrasonic data

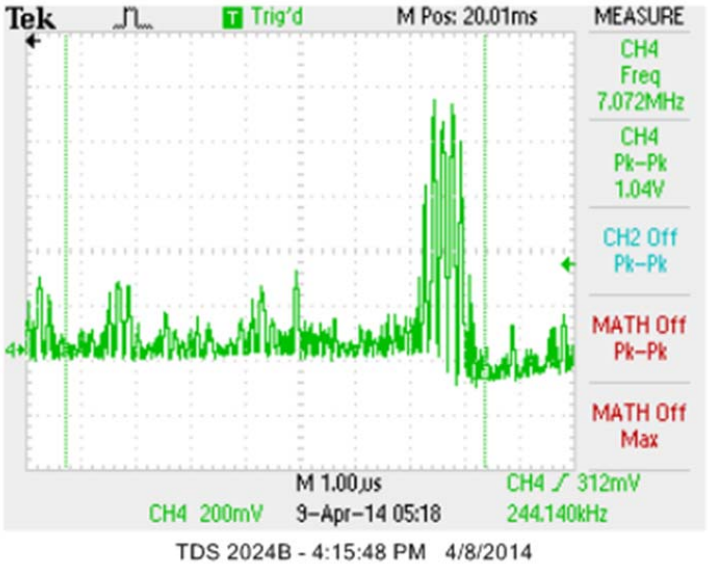

Figure 16. DAC output showing the results of the target detection algorithm

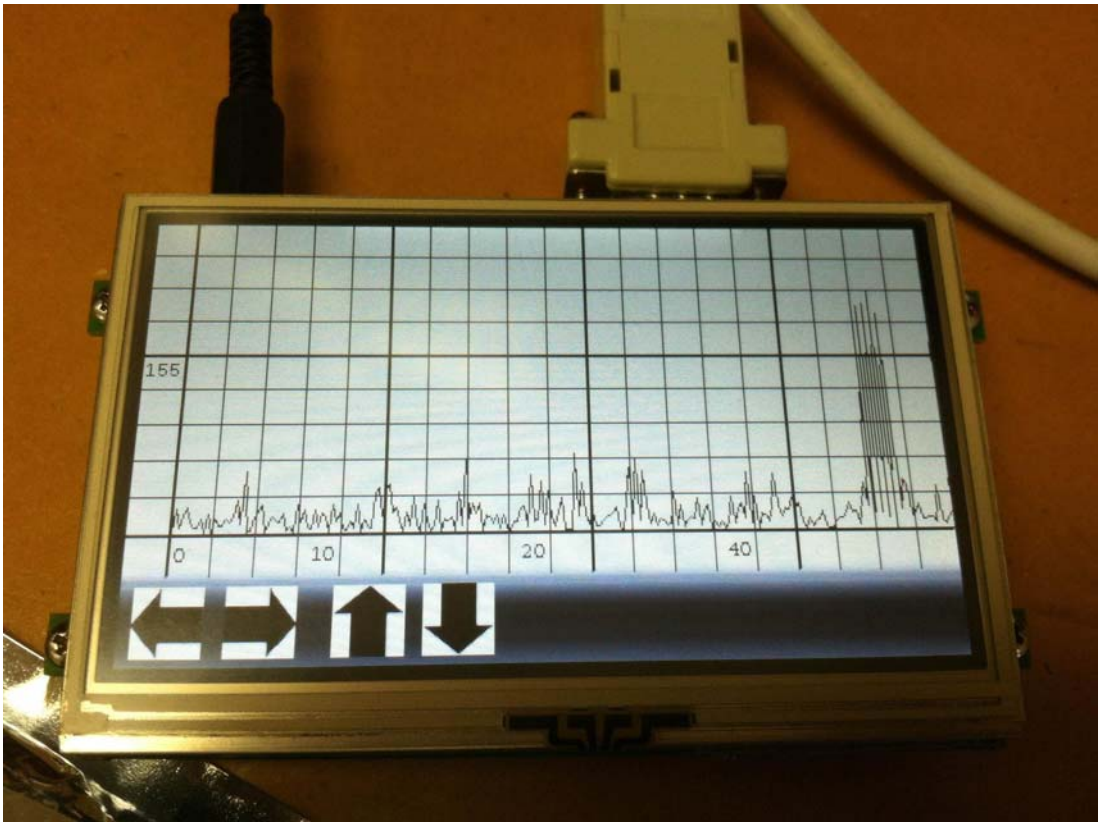

Figure 17. Signal detection displayed on Amulet Touchscreen

Overall, the system works as expected and meets the specifications listed in the proposal. As mentioned in Section II, there are some challenges during the design cycle of project. Since the system runs at 100 MHz sampling rate, it is probably the highest speed signal processing system handled by ECE senior students at Bradley University. When the signal is processed at such high speed frequency, especially it is converted from analog to digital, then digital to analog domain for the purpose of data acquisition; the signal quality becomes not acceptable for signal processing. To solve the problem, differential signals are used in the data acquisition processing. Low-variant differential signals are used to represent the clock for data acquisition. In this way, the noise is greatly reduced so that the signal processing can be done on these raw data.

IV. Conclusion

In this project, a real-time ultrasonic data acquisition platform based on has been implemented. FPGAs are adopted to add the extendibility of the system. The system runs at 100 MSPS for data acquisition and has the ability of LCD display. Most of specifications in the project proposal have been met. More work is needed to do research in efficient implementation of ultrasonic NDE signal processing algorithms. The platform has not only the ability of supporting ultrasonic signal processing research, but also the flexibility of implementing applications in control, communication, and other ECE areas.

V. Acknowledgement

This work is supported in part through by a Research Excellence Award Grant from Bradley University and the Research Seed Grant, Illinois Space Grant Consortium (2013-2014).

VI. Reference

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