OFDM Transceiver using Verilog Proposal

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NOVEMBER 21, 2013
Project Outline

- Orthogonal Frequency Division Multiplexing (OFDM)
- Project Overview
- Project Goals
- Project Description
- Simulations
- Project Status
- Results
- Specifications
- Equipment
- Schedule
OFDM

- Widely Used in digital communication systems
- Low inter-symbol interference
  - Less distortion caused by symbols interfering with subsequent symbols
- Used in Wi-Fi
  - 802.11a, LTE, 4G
- Spectral Efficiency
  - Transmit more data faster in a given bandwidth in presence of noise
How does OFDM work?

• OFDM is based on the concept of frequency-division multiplexing the method of transmitting multiple data streams over a common broadband medium.

• That medium could be radio spectrum, coax cable, twisted pair, or fiber-optic cable.

• Each data stream is modulated onto multiple adjacent carriers within the bandwidth of the medium, and all are transmitted simultaneously.

• An example would be cable TV
  • transmits many parallel channels of video and audio over a single fiber-optic cable and coax cable.
Project Overview

- Implements an Orthogonal Division Multiplexing (OFDM) communication system

**Figure 1: High Level OFDM system**
OFDM Signal

\[ s(t) = \sum_{n=-\infty}^{\infty} \left( \sum_{k=0}^{N-1} X_{n,k} g_k (t - nT_{os}) \right) \]

\[ g_k(t) = \begin{cases} e^{j2\pi f_k t} & \text{if } t \equiv [0,T_{os}] \\ 0 & \text{Otherwise} \end{cases} \]

\[ f_k = \frac{k}{T_{os}} \quad \text{K=0,.........N-1} \]

- The OFDM signal is written as a set of modulated carriers transmitted in parallel
Transmitter and Receiver

• An OFDM signal consist of a sum of orthogonal subcarriers.

• The subcarriers are modulated using QAM modulation.

• The cyclic prefix is used as a guard interval in order to reduce the intersymbol interference. The cyclic prefix will be added after taking the IFFT.

• Parallel-to-serial and serial-to-parallel conversions are required to transmit data through the system.
Project Goals

• The project aims to verify a complete OFDM system using field programmable gate arrays (FPGA) and Verilog hardware description language.
Project Description

• The project is divided into three stages.

  • Stage 1: MATLAB/Simulink

  • Stage 2: Single FPGA board implementation

  • Stage 3: Dual FPGA board implementation and system performance evaluation
Zach Asal
Stage 1: MATLAB/Simulink

- OFDM models will be designed and tested using MATLAB and Simulink
- This stage is used to create a reference system.
MATLAB simulation

- 1 piece of data
- 1 frequency present
- Data looks like 00010...

Figure 3: OFDM after iFFT, one frequency
MATLAB simulation

- 2 pieces of data
- 2 frequencies present
- Data looks like 00010001...

Figure 4: OFDM after iFFT two frequencies
Simulink Model

Figure 5: OFDM Simulink Model

- Channel model
  - \( Y(t) = x(t) \ast h(t) \)
  - Where \( h(t) \) is the impulse response of the channel
Simulink Model

• Model contains transmitter, receiver, and a basic channel model

• Channel model
  • \( Y(t) = x(t) \cdot h(t) \)
  • Where \( h(t) \) is the impulse response of the channel
Simulink results

- When we sent a sound file through the OFDM transceiver with a simple channel model, these were the results

- Input

- Output

Figure 6: Input and Output from Transceiver
Stage 2: single FPGA board Implementation

- Verilog HDL will be used to construct all models in the OFDM system
- Channel effects are not considered
- The whole system will be implemented on a single FPGA board
Stage 3: Dual FPGA board implementation and system performance evaluation

- The transmitter and receiver are implemented on a separate FPGA board using Verilog HDL
- Analog-to-digital converter (ADC) and digital-to-analog converter (DAC) modules are included
- Channel effects degrade the overall system performance
- The system will be measured in terms of bit error rate and compared to theoretical results
Results

• Stage 1: MATLAB/Simulink
• Stage 2: Single FPGA board implementation
• Stage 3: Dual FPGA board implementation and system performance evaluation
Results

• Stage 1: MATLAB/Simulink

• Stage 2: Single FPGA board implementation

• Stage 3: Dual FPGA board implementation and system performance evaluation
Project status

• Starting stage 2
  • Begin writing Verilog code

• Simulink model
  • Only part left is to add a more complex channel model that incorporates noise, so \( y(t) = x(t)h(t) + n(t) \)
  • QAM modulator and demodulator blocks
Paul Pethsomvong
Specifications

- We used the IEEE 802.11a as a guide for our specifications
- 802.11a belongs to the High Speed WLAN category with peak data rate of 54Mbps

<table>
<thead>
<tr>
<th>Specifications</th>
<th>IEEE 802.11a</th>
<th>Chosen Specifications</th>
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<tbody>
<tr>
<td>Channel Bandwidth</td>
<td>5 GHz</td>
<td>5 MHz</td>
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<tr>
<td>Channel Spacing</td>
<td>20 MHz</td>
<td>20 KHz</td>
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<tr>
<td>Symbol Rate</td>
<td>2048Kbits/sec</td>
<td>128 bits/sec</td>
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<tr>
<td>Sub Carriers</td>
<td>1024</td>
<td>32</td>
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<tr>
<td>Sub Carrier Spacing</td>
<td>312.5 K</td>
<td>312.5 Hz</td>
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<tr>
<td>Symbol time</td>
<td>4.88 * 10^-7</td>
<td>7.81 * 10^-3</td>
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<tr>
<td>FFT size</td>
<td>64</td>
<td>16</td>
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</table>

Table 1: Specification list
Equipment

- FPGA board – XtremeDSP Development Kit-IV
  - Includes two ADC and DAC channels
Equipment

• Xilinx software to code Verilog
• Oscilloscope
## Schedule

<table>
<thead>
<tr>
<th>Unique ID</th>
<th>Name</th>
<th>Start Date</th>
<th>Date to be completed</th>
<th>Percent completed</th>
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<tr>
<td>1</td>
<td>Trans: Serial-to-Parallel</td>
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<td>12/8/2013</td>
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<td>5</td>
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<td>1/9/2013</td>
<td>1/16/2013</td>
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<td>1/30/2013</td>
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<tr>
<td>9</td>
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<td>2/6/2013</td>
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<tr>
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<td>Rec: remove cyclic prefix</td>
<td>2/6/2013</td>
<td>2/20/2013</td>
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<tr>
<td>13</td>
<td>Testing/debugging</td>
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<td>15</td>
<td>Combine receiver and transmitter</td>
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<td>3/20/2013</td>
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<td>Complete overall system</td>
<td>3/20/2013</td>
<td>3/27/2013</td>
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</table>

**Figure 7: OFDM TV Schedule of tasks**
Questions?
How does OFDM work

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