# Reconfigurable FPGA Implementation of Digital Communication System (RFIDCS)

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System Block Diagram

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**Introduction**

This project is an attempt to develop various reconfigurable digital communication systems for use on a FPGA programmed in VHDL. The primary goal of this project is to determine whether or not the communication system's transmitter and receiver can be contained on a single FPGA. If not, the goal becomes the identification of what advances are necessary for the FPGA to have this kind of reconfigurable functionality. The initial communication system developed will be an amplitude modulated (AM) system. Based on the results of the AM system, a frequency modulated (FM) system is tentatively scheduled to follow. The Altera UP2 development board contains the FPGA that will be used to implement the communication system design.

**Overall System Flow Diagram**

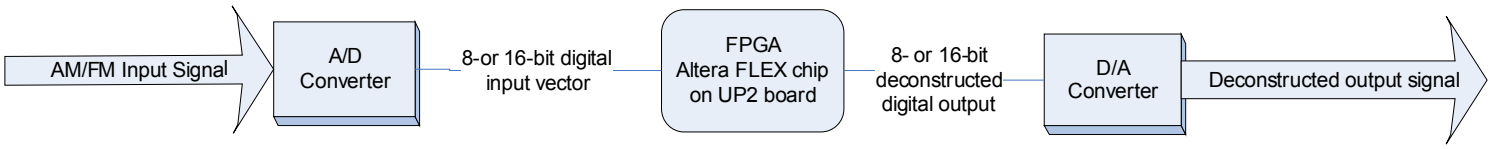


**Figure 1-1** High-level RFIDCS complete system view

**Description of Input and Output Connections among Subsystems**

For the initial system being developed, an AM signal will act as the overall system input. After undergoing an A/D conversion on an external A/D chip, the digital input signal will be read by the FPGA in its receiver configuration. After processing and deconstruction, the signal is then outputted by the FPGA configured as a transmitter to the D/A converter. The output of the D/A converter is the overall system output; a deconstructed equivalent of the AM input signal.

**FPGA**

Figure 2-1 focuses on the flow of data inside the FPGA. A control logic module will be necessary to switch the FPGA between its receiver and transmitter modes. The control logic will also be instrumental during the multiplication process because of the use of the Booth multiplication algorithm, which will be explained later. For this reason, it may be beneficial to have two separately dedicated control modules, one for mode control and one for multiplication data arrangement control.

In receiver mode, the FPGA will read and store the input data from the A/D converter. This data is then multiplied by an internally generated carrier frequency signal. The ideal method for producing this carrier frequency signal (e.g. cosine wave) within the FPGA has yet to be determined and is the subject of upcoming laboratory research. The control logic then switches the FPGA to transmitter mode based on a signal generated signifying the end of the current multiplication process. The product is then transmitted out of the FPGA to the external D/A converter.

**FPGA Data Flow**

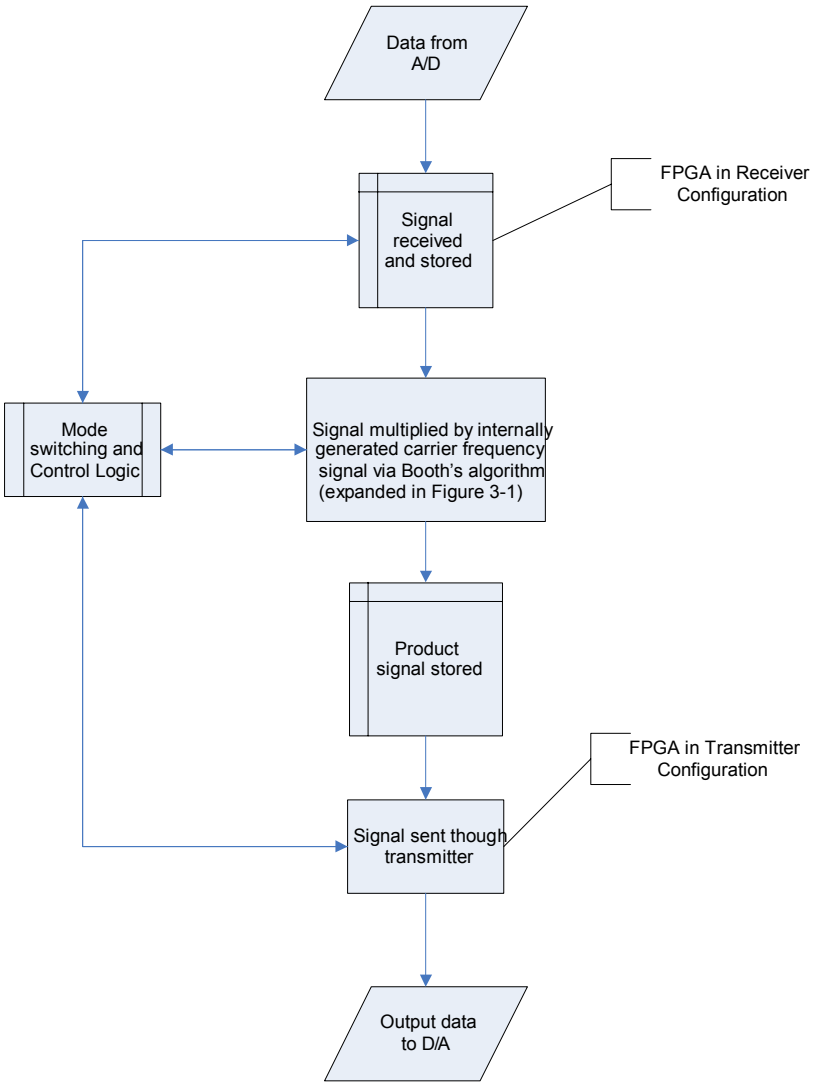


**Figure 2-1** Showing the data flow and necessary code blocks internal to the FPGA

The function of individual blocks in figure 2-1 is discussed below.

**Booth Multiplication Flowchart**

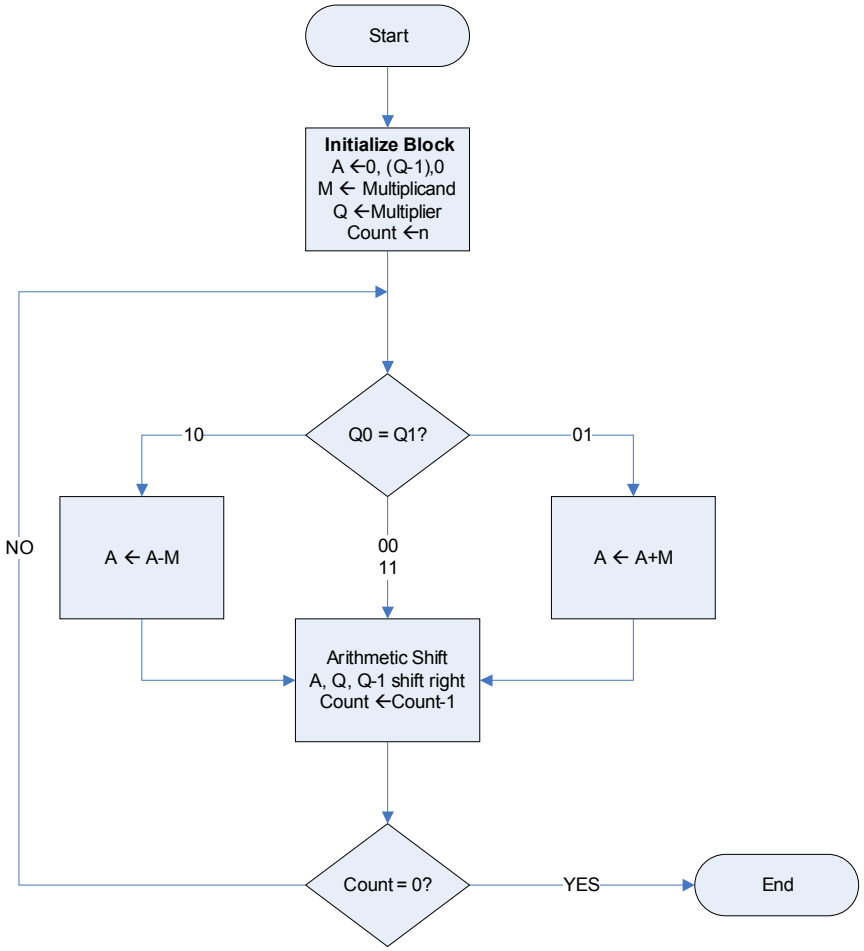


**Figure 3-1** Data flow of the Booth multiplication algorithm

Figure 3-1 expands upon the Booth algorithm multiplication block show in Figure 2-1. The Booth algorithm is a fast and efficient method of two signed two's compliment variables. It is faster than conventional multiplication algorithms because it utilizes the fact that in multiplication, not all bits of the partial product need to be propagated to the next stage of summation. By eliminating the unnecessary bits, the size of the partial products generated is reduced significantly, allowing the next summation to be reached sooner and saving valuable hardware space. A partial schematic of a parallel two's compliment Booth multiplication is shown in Figure 4-1. Variable 'a' is the multiplier and 'b' is the multiplicand. Both are 32-bit two's compliment numbers. The add32csa block performs the addition of the variables 'a' and 'b' and a partial schematic of this block is shown in Figure 4-2. 'a' and 'b' are summed by the fadd block and then transmitted to the next cascaded add32csa segment.

**Booth Multiplication Schematics**

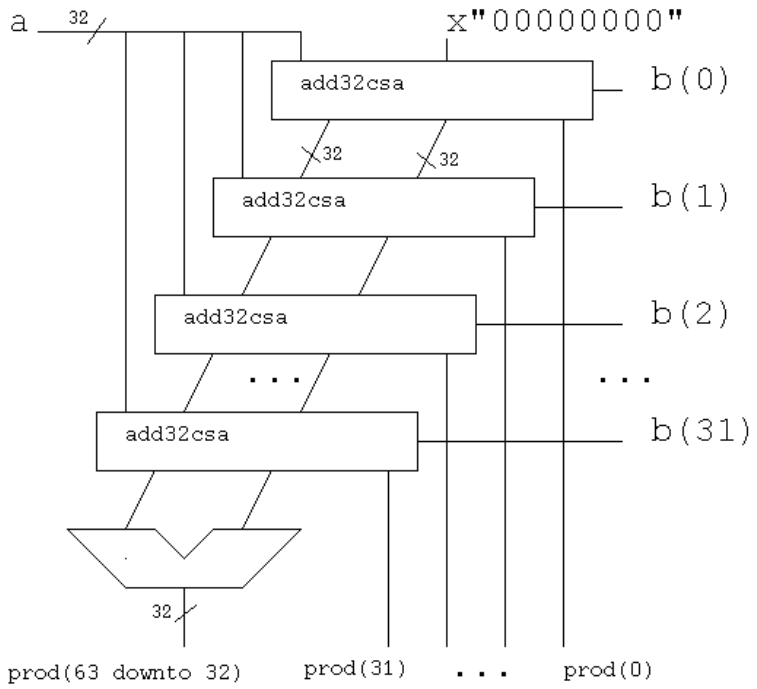


**Figure 4-1** Booth multiplication partial schematic

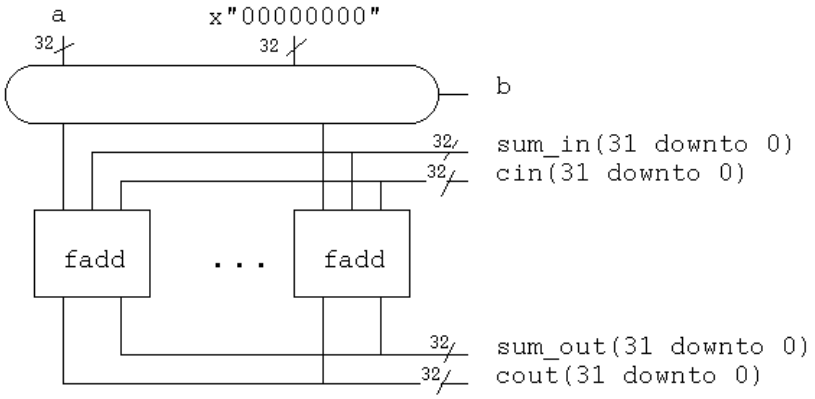


**Figure 4-2** Partial schematic of the add32csa block in shown in figure 4-1

**References**

**[1]** University of Maryland, Department of Computer Science and Electrical Engineering, http://www.csee.umbc.edu/help/VHDL/samples/samples.shtml#mul32