Reconfigurable FPGA Digital Communication System (RFIDCS)

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Functional Description

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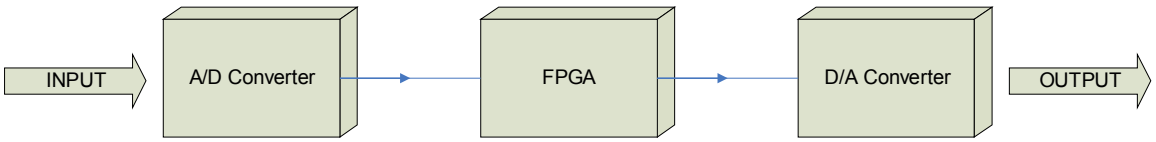
Background

Improvements in the performance and density of FPGAs over the past decade has caused firmware designers to reexamine the role of FPGAs in their end products, specifically relating to the use of reconfigurable FPGAs. Reconfigurable logic design involves manipulation of the logic within the FPGA at run-time. This allows the hardware to change in response to the demands placed upon the system while it is running. Benefits of using a FPGA hardware design over more traditional application specific integrated circuits (ASIC) include greater functionality with a simpler hardware design, lower system cost, and reduced time-to-market. Benefits of using a reconfigurable FPGA in a communication system include reducing the size of the product by including the transmitter and receiver on a single chip, which in turn reduces cost. [1]

Objectives

The objective of this project is to develop various digital communication systems to be implemented on a FPGA programmed in VHDL. The communication system's transmitter and receiver will be contained on a single FPGA, making it a reconfigurable system. The initial communication system developed will be an AM system, with a FM communication system to follow on the same FPGA. The Altera UP2 development board contains the FPGA that will be used to implement the communication system design.

Overall System Flow Diagram



Description of Inputs and Outputs

The inputs and outputs are one in the same for the Reconfigurable FPGA Implementation of Digital Communication System. This means that the receiver and transmitter signals will be read into the reconfigurable FPGA. The system will switch functionality in run-time, so receiver and transmitter signals are treated as both inputs and outputs. The inputs and outputs initially tested will be voice signals, but other communication signals can be implemented using this system. A possible use of this system would be a walky-talky device contained on a single IC.

Bibliography

[1] A Single-Chip Supervised Partial Self-Reconfigurable Architecture for Software Defined Radio – *IEEE Computer Society http://csdl2.computer.org/persagen/DLAbsToc.jsp? resourcePath=/dl/proceedings/ipdps/& toc=comp/proceedings/ipdps/2003/1926/00/1926toc.xml& DOI=10.1109/IPDPS.2003.1213354*