International IOR Rectifier DESIGN TIPS

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MAXIMIZING THE LATCH IMMUNITY OF THE IR2151 & IR2152 IN BALLAST APPLICATIONS

The IR2151 and IR2152 are high voltage integrated circuits (ICs) designed specifically for controlling electronic lamp ballasts. These devices include a front-end oscillator similar to the popular CMOS 555 timer circuit, and a high voltage half-bridge MOS gate driver. Additional circuits control the startup of the IC and the lamp, and provide a nominal 1.2µs cross-conduction dead-time between the high-side and low-side gate driver outputs. The IR2151 and IR2152 differ only in their oscillator-output-to-gate-driver-output phase relationships.

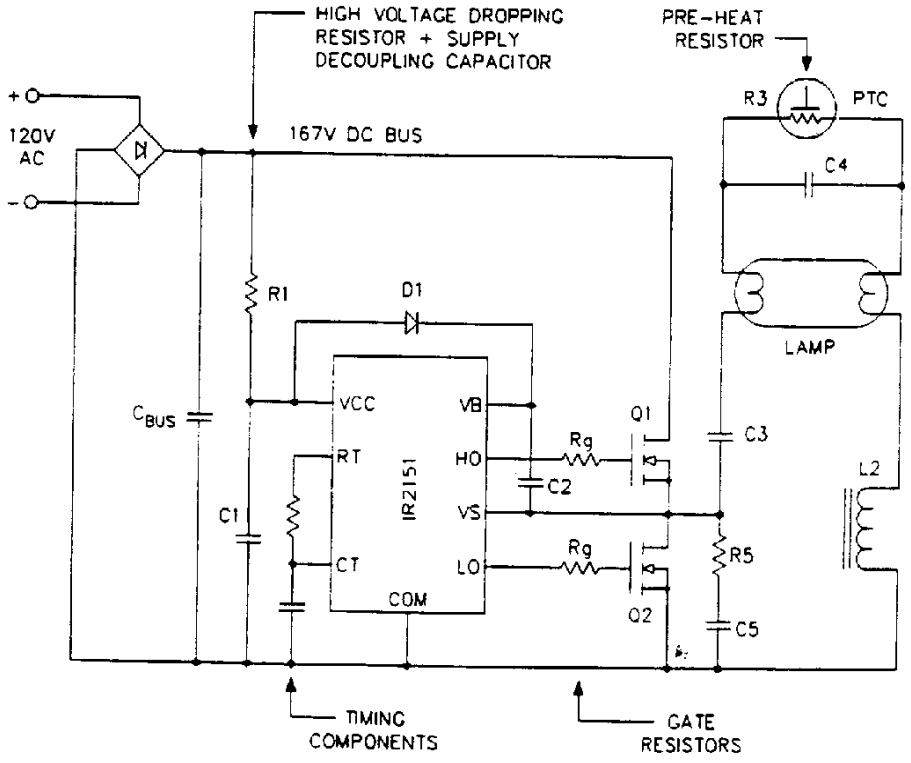

Figure 1 : An Electronic Lamp Ballast Utilizing the IR2151 Controller IC.

Figure 1 illustrates a typical electronic lamp ballast circuit using the IR2151 IC as the central ballast controller. The output of the half-bridge oscillates at a frequency determined by the timing components RT and CT (with a 50% duty cycle), and self-starts when the high voltage dropping resistor R1 charges the IC supply voltage decoupling capacitor C1 above the chip's rising undervoltage lockout (UVLO) threshold (UVCC+). Lamp filament preheating is accomplished by means of the positive temperature coefficient (PTC) resistor R3, which initially has a low value. As this resistor heats up, the voltage across the start capacitor C4 rises, until the lamp has sufficient voltage across it to strike. Once the lamp has struck, its beam current is controlled by the half-bridge output frequency, the dc bus voltage, and the value of the series resonant load filter components C3 and L2.

Understanding the root causes of CMOS gate driver latching is the first important step to preventing such problems from occurring in power half-bridge circuits. Figure 2 illustrates the output stage of a typical CMOS gate driver IC. Although the only intentional active devices in this circuit are the PMOS and NMOS drive transistors (MP1 and MN1), parasitic bipolar NPN and PNP transistors are associated with the active CMOS devices and their ESD protection diodes. To minimize the effects of these parasitic bipolar devices, significant design work occurs in two areas. The first effort is in the layout of the output stage to reduce the base-to-emitter shunt resistance. The second effort is to maximize the component of their total collector current which flows directly to the supply (instead of to the complementary device). The PNPN latch structure, however, cannot be completely eliminated, and as such the SCR formed will turn on under certain conditions.

With respect to the application circuits for the IR2151 and IR2152 ICs, the most common method of triggering the PNPN SCR structure is to force an output either above the supply voltage or below ground by more than a bipolar transistor voltage V_{BE} *and* to have the collector current of this device sufficient to turn on the complementary transistor. When both devices turn on and the product of their Betas exceeds 1.0, regeneration occurs, and the supply is shorted to ground through the SCR structure. This often results in permanent damage to the metallization within the IC and a loss of functionality.

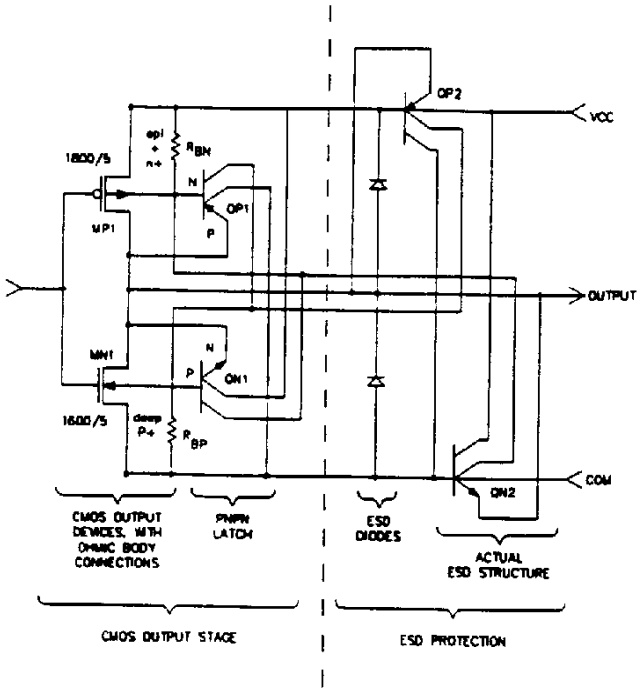

Figure 2 : The CMOS Gate Driver Output Stage, Including Parasitic NPN and PNP Transistors.

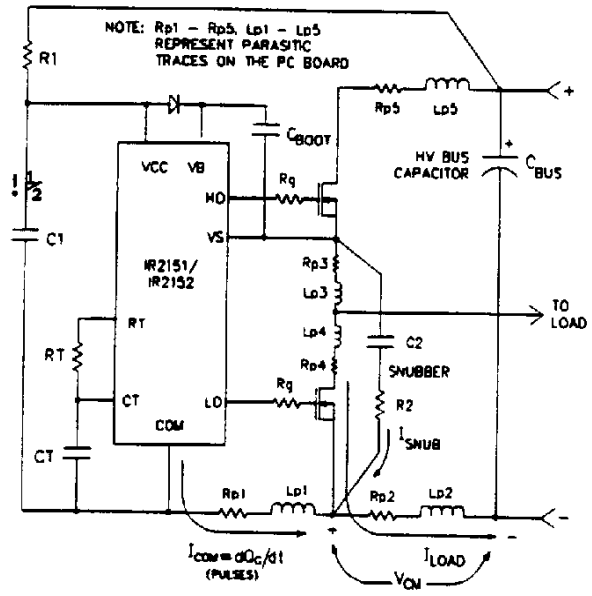

Figure 3a: Proper IC Ground Layout, which Results in common-mode noise.

The IR2151 and IR2152 are specified to have a latch immunity capability of at least 500mA, meaning that if you force an output either above the supply voltage or below the ground potential by means of a 500mA current source, with the supply biased to 12V, that no latching phenomenon will occur (i.e, the PNPN structure does not regenerate). The current required to trigger the latches within the IR2151 and IR2152 typically exceedS 1.2A at room temperature. In addition, due to the low f_T of the parasitic lateral PNP transistor (f_T < 1Mhz), the latching current is also a function of the current pulse width. For current pulse widths below 1µs, the effective latching current rises dramatically, and if the current pulse is short enough, the latch cannot regenerate at all. Finally, the temperature coefficient of the latch current is negative (TC = -5000ppm/°C), due to the positive temperature coefficient of the parasitic NPN transistor's Beta.

Avoiding potential latches within an application circuit which utilizes either the IR2151 or the IR2152 is not difficult if proper design and layout techniques are used.

First, proper grounding techniques should be employed. The IC ground (COM) pin should be tied directly to the source of the low-side power MOSFET/IGBT, and then this point should be routed to the negative terminal of the high voltage bus capacitor (see Figure 3a).

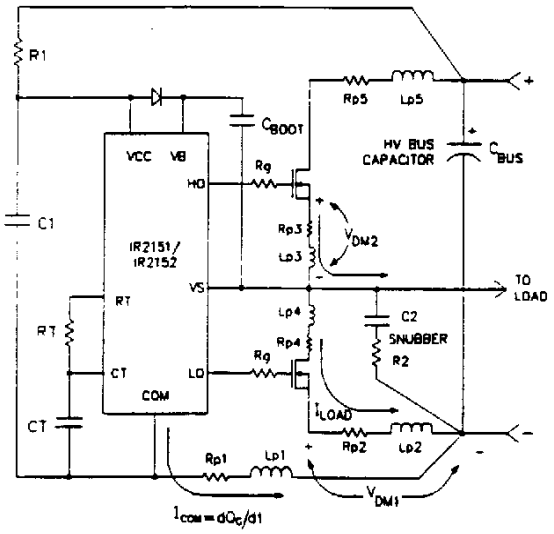

Figure 3b: Improper IC Ground Layout, which Results in Differential Mode Noise.

This results in a common-mode $L_P * di_L/dt$ noise on the IC ground and source of the low-side power MOSFET/IGBT, and reduces the possibility of turning on a latch within the IC (Note: Because the supply pin to the IC is decoupled locally by a capacitor to ground (COM) and decoupled from the power circuit by some resistive impedance, it moves with the low-side power MOSFET/IGBT source in a common-mode fashion also.). This same layout guideline applies to the high-side MOSFET/IGBT and gate driver output HO (and its return path to VS) as well. If the pc board layout is similar to that shown in Figure 3b, however, the differential-mode $L_P * di_L/dt$ noise could cause the LO (or HO) terminal to be forced below the COM (or VS) pin, making the circuit more latch-prone.

The second latch immunity design issue to be considered regards displacement currents which flow out of the IC during output voltage switching, and the effective ac impedance on the gate of the power MOSFET/IGBT.

Referring to Figure 4, the output voltage dV/dt (which is negative), multiplied by the gate-to-drain capacitance of the low-side power MOSFET/IGBT, creates a displacement current which flows out of the IC, forcing the LO output voltage below the ground potential (COM).

If this displacement current is high enough, the parasitic gate driver output stage NPN and PNP transistors will turn on, triggering a VCC-to-COM latch. This SCR structure will then attempt to discharge the local supply-to-ground decoupling capacitor through the internal VCC and COM metal connections within the IC. But as the typical CMOS output stage parasitic SCR is capable of conducting several amps of current, the latching current often exceeds the fusing current of the metal connections within the IC, and the supply to the IC effectively becomes an open circuit. The situation is worsened by the fact that the local IC low voltage decoupling capacitor should exhibit a low ESR in order to establish a low ac impedance on the supply to the IC, and as such is capable of delivering high peak currents to the SCR.

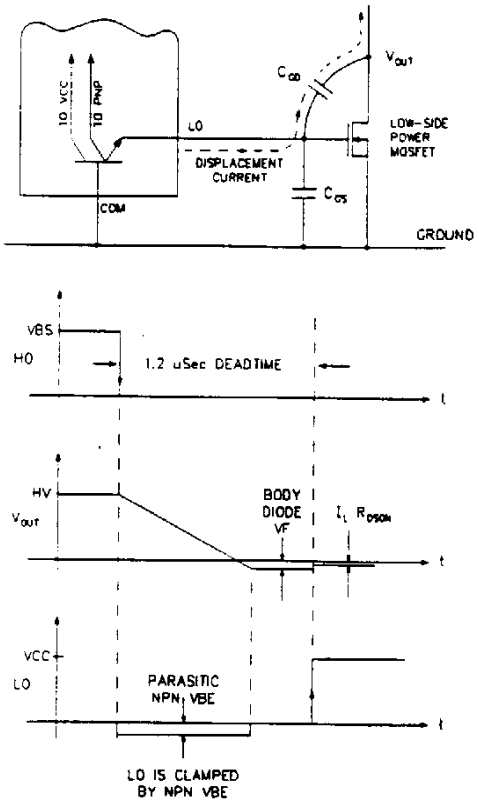

Figure 4 : Output Voltage Slewing-Induced IC Displacement Currents.

The ballast designer should note here that a compromise must be reached between conduction and switching losses in the power MOSFETs/IGBTs, and that what is normally considered "conservative" design (i.e., using oversized power MOSFETs) can lead to other problems.

One method of reducing the effect of these $C_{GD} * dV_{OUT}/dt$ displacement currents, and thereby increasing the latch immunity of the gate-driver-IC-to-power-transistor system, involves placing a snubber from the half-bridge output to either the high voltage dc bus or the ground return line. Referring to the ballast schematic shown in Figure 5, the 10Ω, 0.001μF RC snubber from the half-bridge output node to ground will reduce the output dV/dt, thereby reducing the peak displacement currents flowing out of the IC (such a snubber also serves to reduce EMI noise radiated by the ballast). An upper limit for the time constant of the snubber exists, however, because of the 1.2μs dead-time within the IC, and the need to maintain zero-voltage switching operation for the power MOSFETs/IGBTs. It is unlikely, therefore, that a snubber circuit alone will be able to eliminate latching problem for *all* possible IC/MOSFET/Load combinations.

A second method of increasing the latch immunity of the IC/MOSFET/Load system involves connecting a resistor between the IC output (LO/HO) and the gate of the respective power transistor, as shown in Figure 6. This resistor limits the currents which flow out of the IC outputs during half-bridge output voltage transitions, and forces most of the $C_{GD} * dV_{OUT}/dt$ displacement current to flow out of the power MOSFET gate-to-source capacitance. The value of this gate resistor should be chosen to guarantee that the reverse IC output currents never exceed +/-500 mA. [Please note that for normal MOSFET turn-on and turn-off, the output current does not need to be limited; in this mode, the gate resistor serves only to dampen the LC tank circuit associated with the power MOSFET gate-to-source capacitance and gate and source inductances, and to provide the user a means of "shaping" the gate rise and fall times].

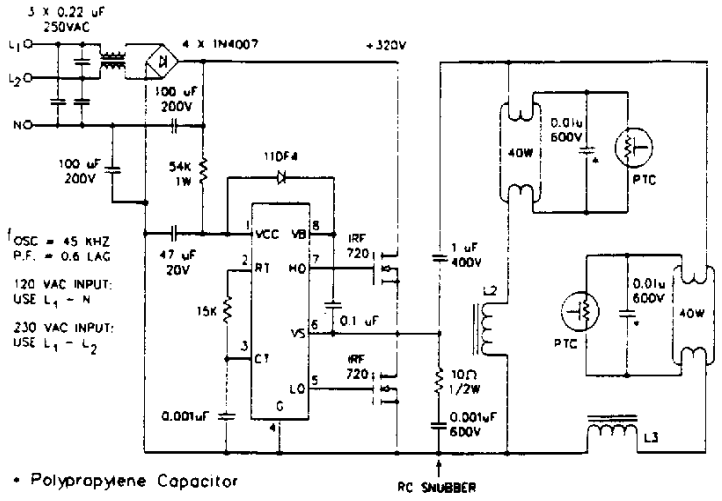

Figure 5: Half-Bridge Output Voltage Snubber Circuit

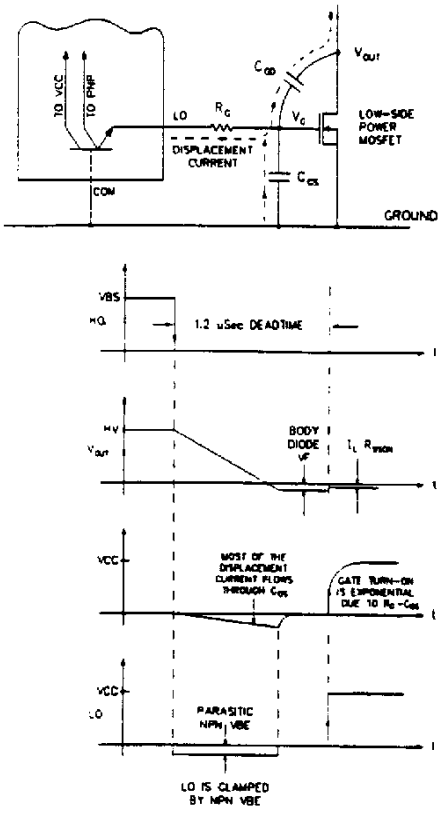

Figure 6 : A Gate Resistor Buffers the IC from Power MOSFET/IGBT Switching Noise.

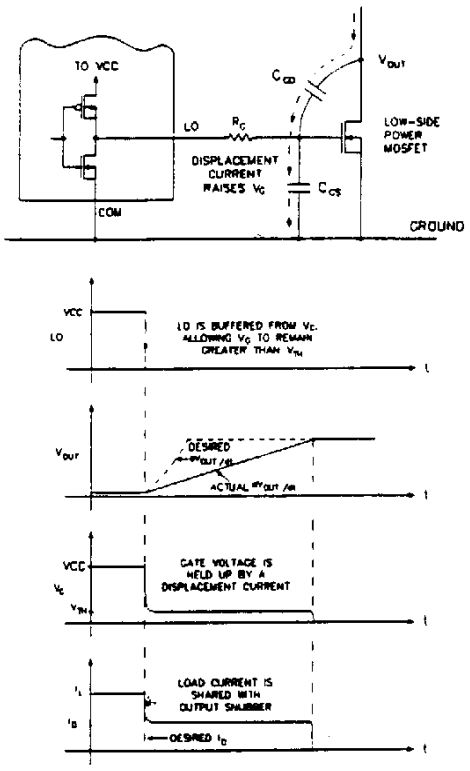

Figure 7: Power MOFET Self Turn-On Due to a High Gate Resistor Value.

An upper limit for the value of this gate resistor does exist, however, that, because of the phenomenon illustrated in Figure 7. If the gate resistor value is too high, then during the positive output voltage transition the C_{GD} * dV_{OUT}/dt displacement current will cause the voltage at the gate of the power MOSFET to exceed its threshold voltage, turning it back on. In this case the output voltage slew rate would be limited by the slow turn-off of the power MOSFET (and not the snubber component values), and switching losses in these power transistors would increase.

For ballast designers who need to have a high-valued gate resistor, this self-turn-on problem can be circumvented by connecting a diode in parallel with the gate resistor, as shown in Figure 8.

The diode is reverse-biased during gate charging, and hence the gate voltage rise time will be determined by the R_G * C_{iss} time constant. During gate discharging, however, the diode is forward-biased, and provides a lower impedance path for faster gate voltage fall times. In addition, the diode is reverse-biased when the C_{GD} * dV_{OUT}/dt displacement currents flow out of the IC output, thereby maintaining good latch immunity.

As a result of all of these considerations, the ballast designer needs to consider the following design parameters somewhat concurrently in order to achieve good IC/MOSFET/Load system latch immunity, good ballast EMI performance, and low switching losses:

1. The size of the power MOSFET/IGBT used and its internal terminal capacitances, which are outlined in the data sheet,
2. The snubber component values and desired output dV/dt,
3. The IC's internal deadtime of 1.2μs, and
4. The gate resistor value.

For additional information regarding either the IR2151 or IR2152 products, or International Rectifier's MOS Gate Driver Power ICs in general, please refer to Application Notes AN-995, AN-973, and AN-978A, and Design Tips DT 92-1 and 94-3.

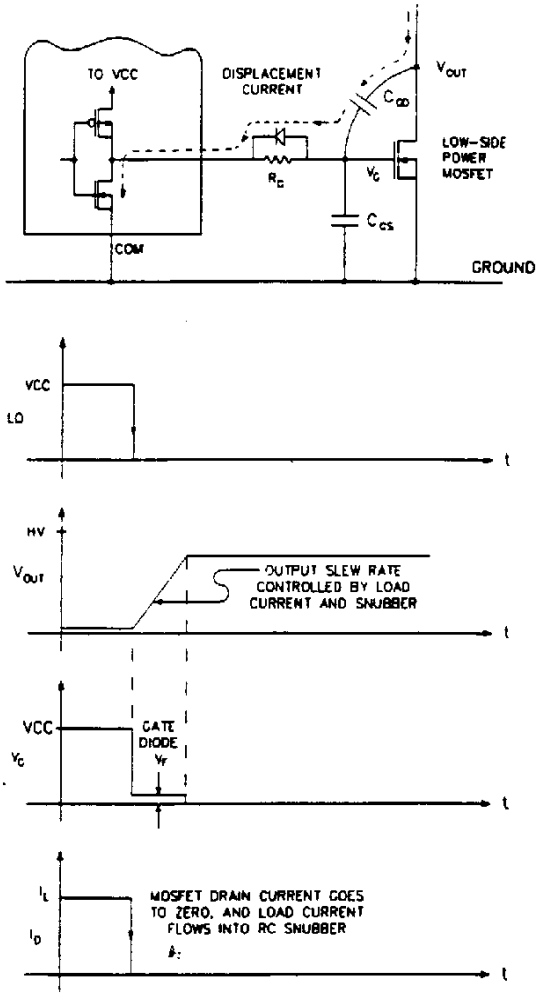

Figure 8: A Diode-Resistor Combination for Slow Gate Turn-On and Fast Gate Turn-Off.