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Patents/Standards/Bibliography

Patents:
www.patents.ibm.com:

boolean search for matrix AND vector AND cmos yielded:

US05475695	12/12/1995	Automatic failure analysis system
US05822608	10/13/1998	Associative parallel processing system
US05761523	06/02/1998	Parallel processing system having asynchronous SIMD processing and data parallel coding
US05752067	05/12/1998	Fully scalable parallel processing system having asynchronous SIMD processing
US05734921	03/31/1998	Advanced parallel array processor computer package
US05636229	06/03/1997	Method for generating test patterns to detect an electric short circuit, a method for testing electric circuitry while using test patterns so generated, and a tester device for testing electric circuitry with such test patterns
US05553002	09/03/1996	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, using milestone matrix incorporated into user-interface

Boolean search for integrated circuit AND cmos AND matrix yielded 105 entries. Most significant ones listed:

US04928265	05/22/1990	Semiconductor integrated circuit
US05400262	03/21/1995	Universal interconnect matrix array
US05781033	07/14/1998	Logic module with configurable combinational and sequential blocks
US05767544	06/16/1998	Semiconductor integrated circuit device
US05675548	10/07/1997	Semiconductor integrated circuit having logic gates
US05668770	09/16/1997	Static memory cell having independent data holding voltage
US05610833	03/11/1997	Computer-aided design methods and apparatus for multilevel interconnect technologies
US05610534	03/11/1997	Logic module for a programmable logic device
US05388065	02/07/1995	Semiconductor integrated circuit
US05341383	08/23/1994	Circuit arrangement suitable for testing cells arranged in rows and columns, semiconductor integrated circuit device having the same, and method for arranging circuit blocks on chip
US05309371	05/03/1994	Method of and apparatus for designing circuit block layout in integrated circuit
US05157627	10/20/1992	Method and apparatus for setting desired signal level on storage element
US05146428	09/08/1992	Single chip gate array
US05726995	12/15/1994	Method and apparatus for selecting modes of an integrated circuit

US4975641	04/21/1989	Integrated circuit and method for testing the integrated circuit
US4902917	01/05/1989	Integrated circuit having mode selection
US4701920	10/20/87	Built-in self-test system for VLSI circuit chips

Applicable patents to our project:

US4902917 01/05/1989 Integrated circuit having mode selection

Abstract:

The mode of operation of an integrated circuit capable of several modes of operation is determined by at least one signal applied to one or more mode selection terminal pins. The signal applied is a selected one of at least two signals derived from a clock signal used by the integrated circuit in its operation. The clock signal is generated by an oscillator which may be included in the integrated circuit or external to it; in either case, the clock signal appears at another terminal pin of the integrated circuit.

Claim:

An integrated circuit having at least two different modes of operation selected by a mode selection circuit in response to one or more inputs applied to one or more mode selection terminal pins, respectively, and one or more other terminal pins for one or more clock signals from a clock means, respectively, wherein at least one mode selection terminal pin is connected to a synchronous decoding circuit responsive to a clock signal related to that applied to the other terminal pin or one of the other terminal pins by the clock means and capable of producing a particular output only when another signal related to the clock signal applied to the said other terminal pin by the clock means is applied to the mode selection terminal pins, the mode selection circuit being responsive to the particular output of the synchronous decoding circuit.

US4975641 04/21/1989 Integrated circuit and method for testing the integrated circuit

Abstract:

An integrated circuit which can be operated in a test mode includes a test input terminal for instructing the switching between an actual use mode and a test mode, a plurality of input terminals, an AND gate for performing logic operations on the input signals from the input terminals, a plurality of flip-flops for storing each of the input signals from the remaining plurality of input terminals by using the output of the AND gate as a timing signal, a decoder for producing a test mode designating signal to select one test mode from a plurality of test modes in response to each of the outputs of the flip-flops, and a control circuit for operating a processing circuit in the test mode designated by the test mode designating signal in response to the test mode setting signal from the test input and the test mode designating signal from the decoder. The configuration of this circuit

permits the testing of the signals from the output terminals of the integrated circuit without excessively increasing the number of input terminals necessary for the test mode.

Claim:

What is claimed is:

1. An integrated circuit comprising:

(a) a test input terminal for receiving a mode signal which switches between an actual use mode and a test mode; and

(b) test mode setting means for setting one of a plurality of test modes, said test mode setting circuit including,

(b1) means for developing a timing signal for logic operations performed on a plurality of first input signals of the integrated circuit,

(b2) a memory for storing a signal from a second plurality of input terminals of the integrated circuit in response to said timing signal, and

(b3) a decoder for developing a signal which sets one of the plurality of test modes.

US4701920 10/20/87 Built-in self-test system for VLSI circuit chips

Abstract:

An improved built-in self-test system fabricated on an LSI circuit chip for performing dynamic tests of main logic function operation. The built-in self-test system includes a control register comprising a series of static flip-flops connected for serial test data transfer and for producing test system control signals. An input shift register connected for serial test data transfer with the control register and for parallel test data transfer with the main logic function is formed by a series arrangement of static flip-flops. An output register connected for serial test data transfer with the input register, and for parallel test data transfer with the main logic function, is formed by a series arrangement of static flip-flops. A test clock enable signal is latched by a test clock enable latch, and gated with a system clock signal to produce input and output register clock signals. A test strobe signal is latched by a test strobe latch and strobed by a flip-flop for use as a control register enable signal. The latched test strobe signal and the latched test clock enable signal are gated with the system clock signal for use as a control register clock signal. A test data output multiplexer decodes a test data select signal produced by the control register and supplies test data represented thereby to a test data output pin.

Claim:

What is claimed is:

1. An LSI circuit including:

main logic function means for performing digital logic operations; and

built-in test system means interconnected with the main logic function means for performing dynamic tests of main logic function operation, the built-in test system means including:

test data input means for receiving test data in a serial format;

clock input means for receiving a clock signal which switches between first and second logic states; and

shift register means responsive to the test data input means and the clock input means for storing and serially transferring test data, the shift register means comprising a series of static flip-flops which enable data stored therein to be maintained irrespective of the logic state of the clock signal.

Standards:

www.nssn.org:

SOAR-3	Title: IC Quality Grades: Impact on System Reliability and Life Cycle Cost
MIL-I-48632(2)	INTEGRATED CIRCUIT, DIGITAL, CMOS CONTROL AND TIMING BASE, MONOLITHIC, SILICON
MIL-I-48634(3)	INTEGRATED CIRCUIT, DIGITAL, CMOS LOGIC ARRAY MONOLITHIC SILICON
IEC 60748-2 Ed. 2.0b	Title: Semiconductor devices - Integrated circuits - Part 2: Digital integrated circuits
IEC 60748-2-10 Ed. 1.0 b	Title: Semiconductor devices - Integrated circuits - Part 2: Digital integrated circuits
IEC 60191-5 Ed. 2.0b	Title: Mechanical standardization of semiconductor devices - Part 5: Recommendations applicable
IEC 60191-3 Ed. 1.0b	Title: Mechanical standardization of semiconductor devices. Part 3: General rules for the
1181-1991	Title: IEEE Recommended Practice for Latchup Test Methods for CMOS and BiCMOS Integrated-
IEC 60747-1 Ed. 1.0 b	Title: Semiconductor devices - Discrete devices - Part 1: General
IEC 60748-1 Ed. 1.0 b	Title: Semiconductor devices. Integrated circuits. Part 1: General
MIL-M-63530(1) NOT 1	MICROCIRCUIT, DIGITAL, CMOS (LOGIC)
MIL-I-48634(3) NOT 1	INTEGRATED CIRCUIT, DIGITAL, CMOS LOGIC ARRAY MONOLITHIC SILICON
MIL-M-38510/765(2) NOT 1	MICROCIRCUITS, DIGITAL, ADVANCED CMOS, SHIFT REGISTERS, MONOLITHIC SILICON, POSITIVE LOGIC
MIL-M-38510/756A(1) NOT 1	MICROCIRCUITS, DIGITAL, ADVANCED CMOS, FLIP-FLOPS, MONOLITHIC SILICON, POSITIVE LOGIC
MIL-M-38510/752B NOT 1	MICROCIRCUITS, DIGITAL, ADVANCED CMOS, AND GATES, OR GATES, MONOLITHIC SILICON, POSITIVE L
MIL-M-38510/750A(1) NOT 1	MICROCIRCUITS, DIGITAL, ADVANCED, CMOS, NAND GATES, MONOLITHIC SILICON, POSITIVE LOGIC

MIL-M-38510/665 NOT 1	MICROCIRCUITS, DIGITAL, HIGH SPEED, CMOS, SHIFT REGISTER, MONOLITHIC SILICON
MIL-M-38510/656(2) NOT 1	MICROCIRCUITS, DIGITAL, HIGH SPEED, CMOS, FLIP-FLOPS MONOLITHIC SILICON
MIL-M-38510/653A(2) NOT 1	MICROCIRCUIT, DIGITAL, HIGH SPEED, CMOS FLIP-FLOPS, MONOLITHIC SILICON, POSITIVE LOGIC
MIL-M-38510/652A NOT 1	MICROCIRCUITS, DIGITAL, HIGH SPEED, CMOS, AND GATES, OR GATES, MONOLITHIC SILICON, POSITIV
MIL-M-38510/650A NOT 1	MICROCIRCUITS, DIGITAL, HIGH SPEED, CMOS, NAND GATES MONOLITHIC SILICON, POSITIVE LOGIC
MIL-M-38510/172B(1) NOT 1	MICROCIRCUITS, DIGITAL, CMOS, AND-OR-INVERT, EXCLUSIVE-OR, EXCLUSIVE-NOR GATES, MONOLITHIC
MIL-M-38510/171B(1) NOT 1	MICROCIRCUITS, DIGITAL, CMOS, OR GATES, MONOLITHIC SILICON, POSITIVE LOGIC
MIL-M-38510/170B(1) NOT 1	MICROCIRCUITS, DIGITAL, CMOS, AND GATES, MONOLITHIC SILICON, POSITIVE LOGIC

Bibliography

Mead, C. (1980). Introduction to vlsi systems. Reading, MA: Addison-Wesley Publishing Co.

Uyemura, J. (1995). Physical Design of CMOS Integrated Circuits Using L-Edit. Boston, MA: PWS Publishing Company.

Prasad, V. EE561 and EE563, and L-Edit working gate designs.