

The following page shows the system level block diagram for our senior project, a matrix-vector multiplier. The circuit multiplies a 3 bit by 3 bit matrix with a 3 bit vector. The output is a 6 bit vector, with 2 bits for each vector element. The circuit also contains a sequence generator to simulate input for testing purposes, and a control signal to switch between testing and normal operation, and a clock signal for the shift registers and flip-flops. The mathematical representation of the circuit looks like this:

$$\begin{pmatrix} A1 & A2 & A3 \\ B1 & B2 & B3 \\ C1 & C2 & C3 \end{pmatrix} \begin{pmatrix} X1 \\ X2 \\ X3 \end{pmatrix} = \begin{pmatrix} Y11 & Y10 \\ Y21 & Y20 \\ Y31 & Y30 \end{pmatrix}$$

$$Y1 = A1*X1 + A2*X2 + A3*X3$$

$$Y2 = B1*X1 + B2*X2 + B3*X3$$

$$Y3 = C1*X1 + C2*X2 + C3*X3$$

Y10 is the sum bit, and Y11 is the carry bit.

Matrix Input Subsystem:

The Matrix Input subsystem contains the values of the matrix being multiplied. There are more than 3 elements to each register, because there will need to be a pause between inputs. The inputs are sent to the processor cells, which require a one clock-cycle delay for processing before receiving the next input. There is also a delay before the first element goes to the processor, in order to synchronize the vector input bit with the correct matrix input bit and output bit.

Input Vector Subsystem:

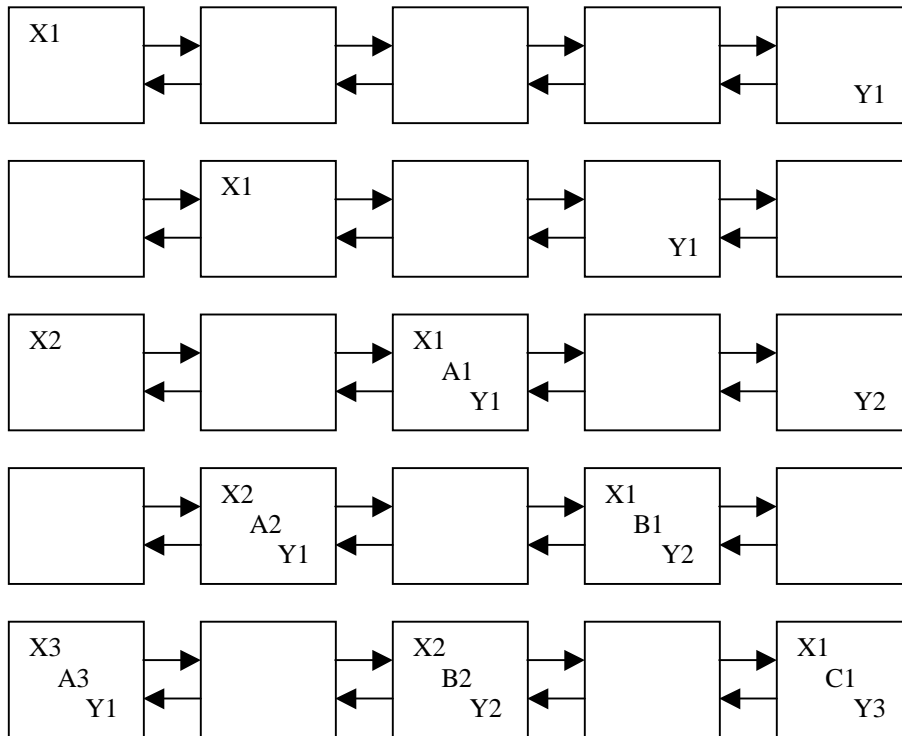
The Input Vector is a shift register, which contains the 3 bit vector that is to be multiplied with the matrix. The inputs are fed into the processors, along with the matrix inputs and the outputs.

Output Shift Register Subsystem:

The Output Shift Register Subsystem consists of the shift register where the final 6-bit answer will be stored.

Processors:

The processors are the five cells between the shift registers. They take the matrix input bit and multiply it with the vector input bit, and add that value to the previous value. An example of the first few clock cycles is shown:



At each step, X and A are multiplied together, and that result is added to the current Y. After this clock cycle, the correct Y1 will be output to the Output Shift Register. Y2 will be output in three more clock cycles, and Y3 will be output in five more clock cycles.

Sequence Generator:

The sequence generator is for use in the testing mode of the circuit. The sequence generator sends predetermined inputs to the matrix and vector parts, so that the output can be compared to expected output. The sequence generator will be added in only if there is enough space on the chip for it.

